

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG ,CPU-Memory	3,4
CPU-Power/CPU-GND	5,6
SO_DDRIII DIMMA1&SO_DDRIII DIMMB1	7,8
LYNX-PCIE/DMI/CLK/USB20&30	9
LYNX-SATA/HOST/GPIO/VGA/CMOS	10
LYNX-SMB/LPC/AUDIO/RTC/SPI	11
LYNX-POWER/GND/Strap	12,13,14
PCIE Slot	15,16
AUDIO 892	17
LAN-RTL8111G	18
DVI Connector	19
HDMI Connector	20
Display port Connector	21
VGA Connector	22
SATA Connector	23
USB3.0 Connector /USB Charger / USB2.0	24,25,26
SIO-NTC6779D/PS2	27
FAN	28
ATX F_Panel/EMI/TPM	29
ACPI Controller UPI	30
VRM12 .5 - ISL95812	31
ISL6208B 3-Phase+MOS CPU	32
UP1504S - DDR POWER	33
OP+MOS - PCH POWER	34
ME POWER	35
XDP / Manual Parts	36,37
EMI CAP	38

# MS-7823

mATX

Ver: 12(243.84x243.84)

## Intel -SharkBay platform Z87

### CPU:

Haswell LGA1150

### System Chipset:

Lynx Point Z87 co-lay H87 & B85

### Onboard Chip:

HD Audio Codec:ALC892

LAN-RTL8111G

SIO:Nuvoton 6779D

Flash ROM: SPI 64 MB/128MB

### Main Memory:

DDRIII (1066/1333/1600MHz) \* 4  
(Dual Channel)

### ACPI:

UPI

### Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1 ) Slot \* 2

PCI Express (X4 ) Slot \* 1

### PWM:

ISL95812 3 Phase

### Other:

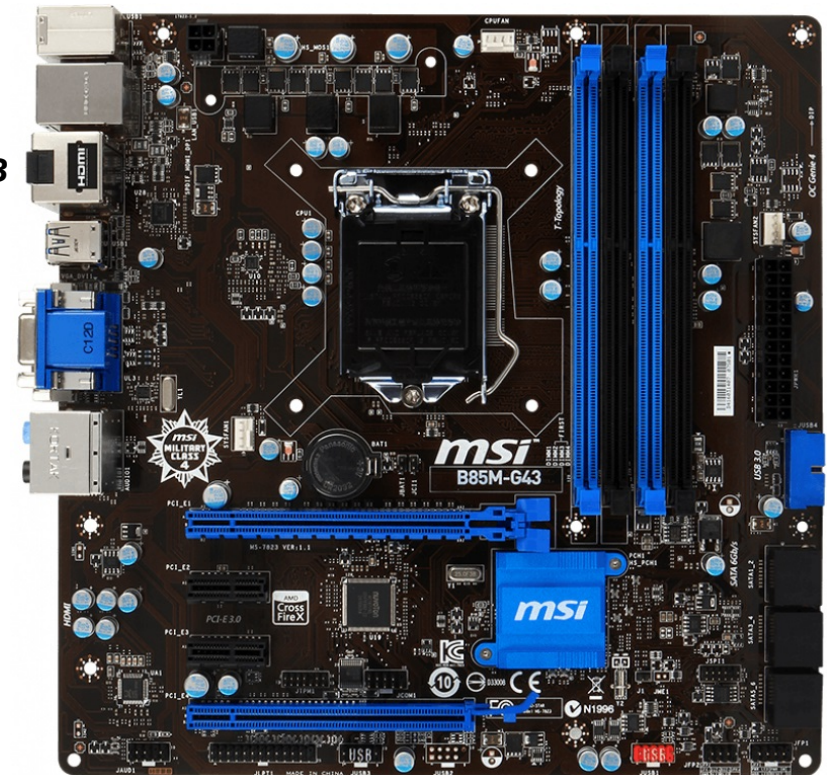
SATA3.0 x6(PCH)

REAL USB2.0 \*4

FRONT USB2.0 \*6

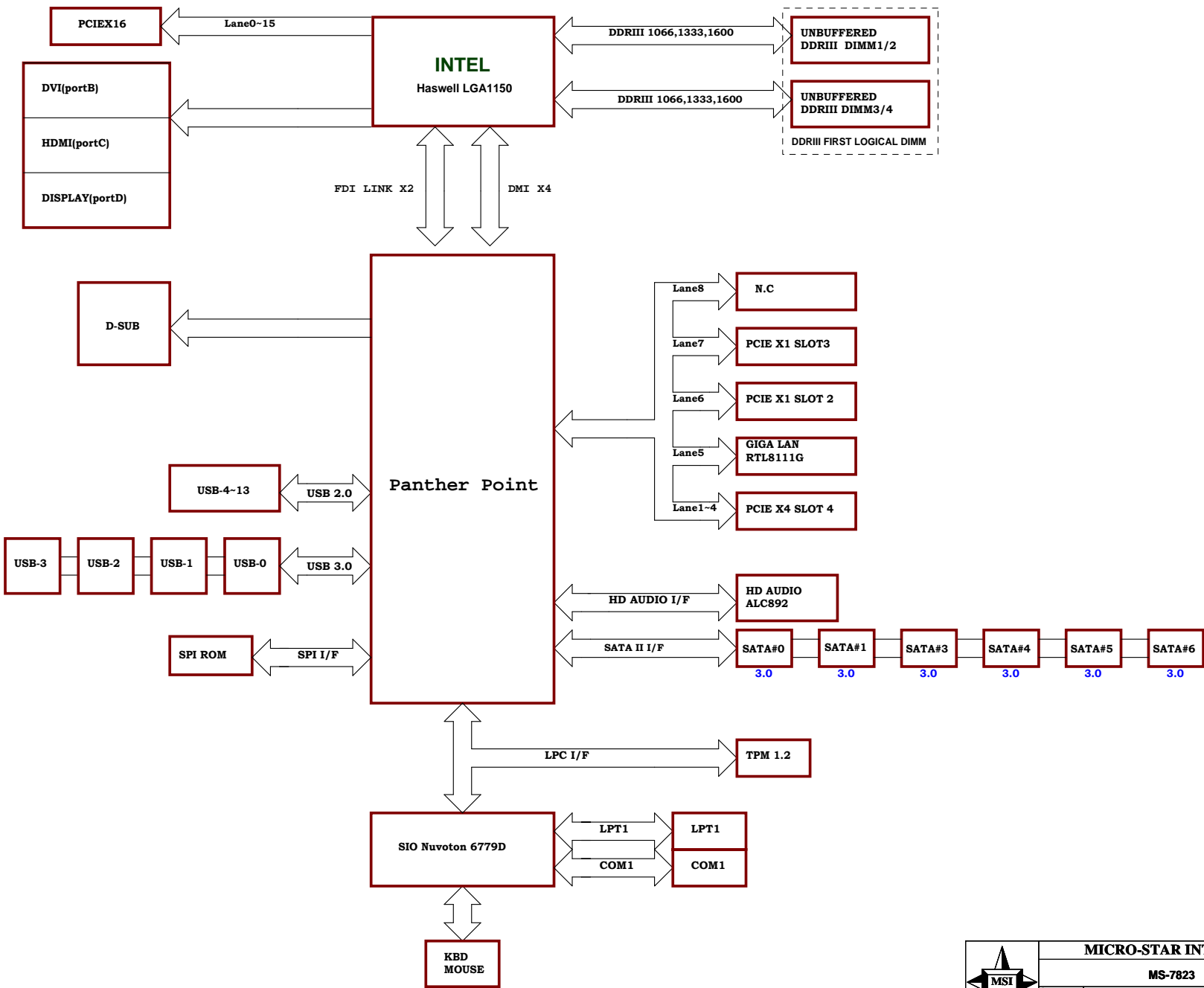
REAL USB3.0 \*2

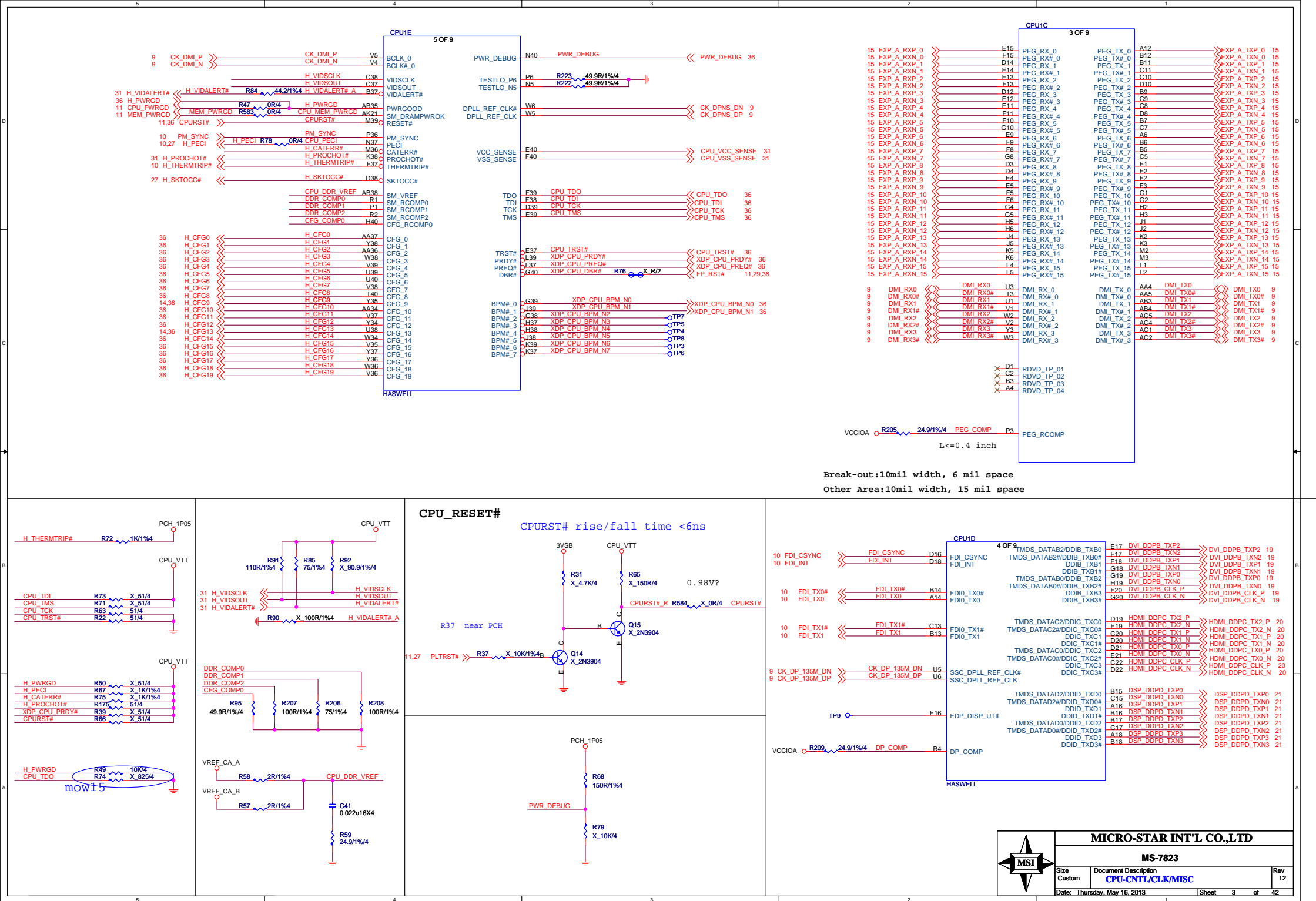
FRONT USB3.0 \*2

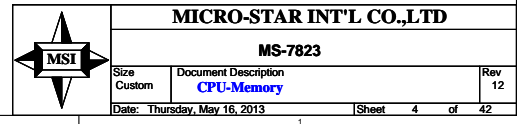


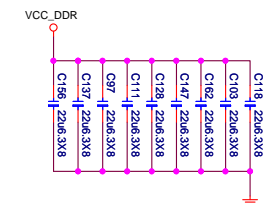
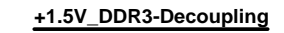
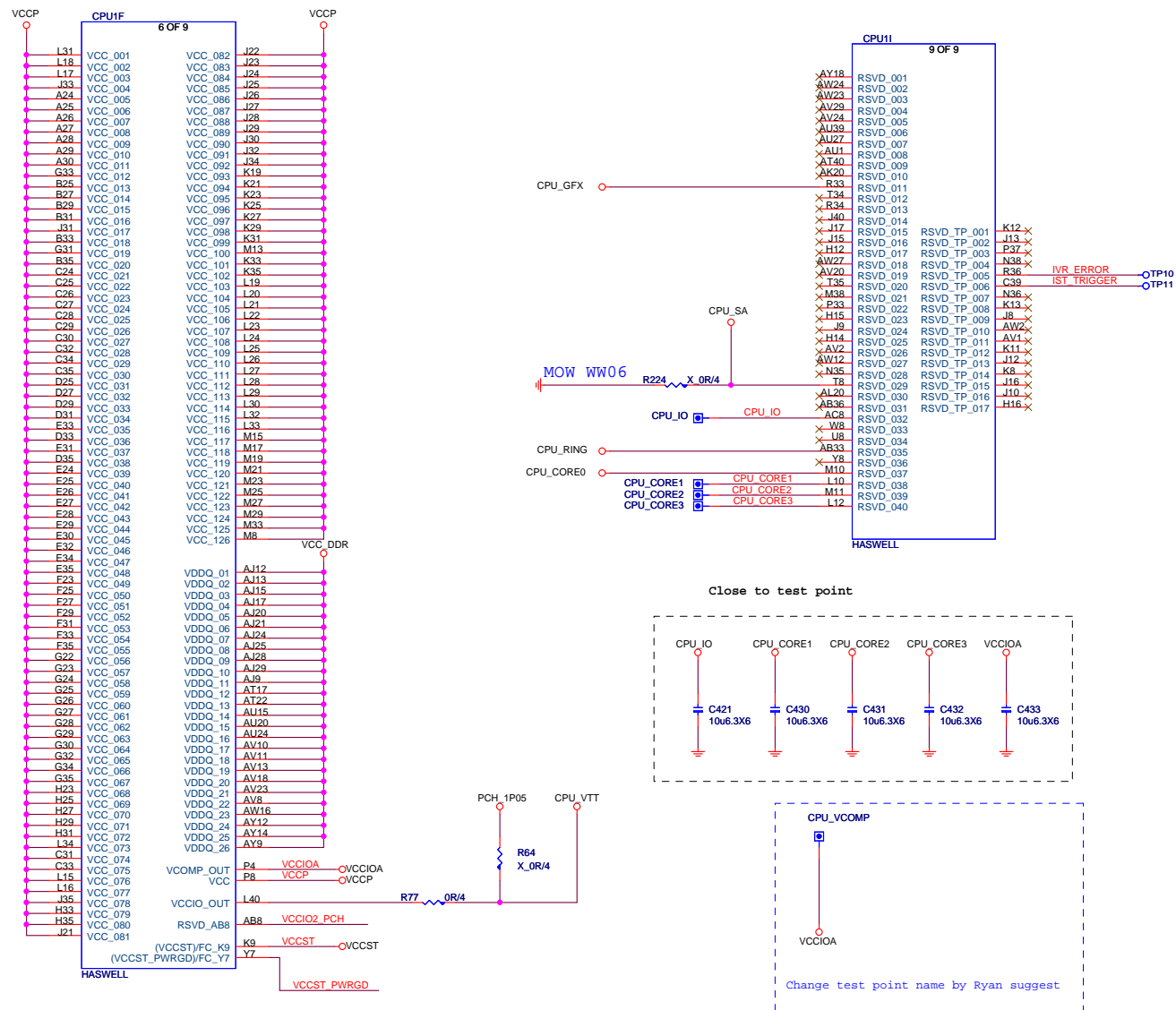
MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size	Document Description	Rev
Custom	Cover Sheet	12
Date: Thursday, May 16, 2013	Sheet 1 of 42	

MS-7823 Block Diagram

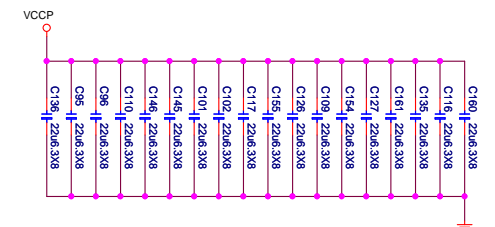






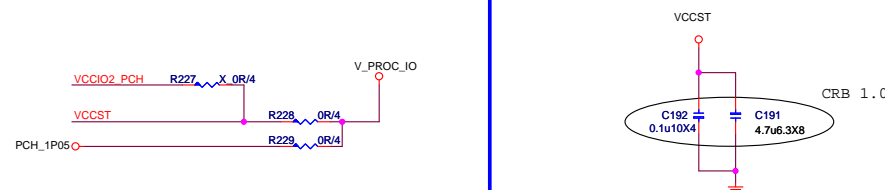
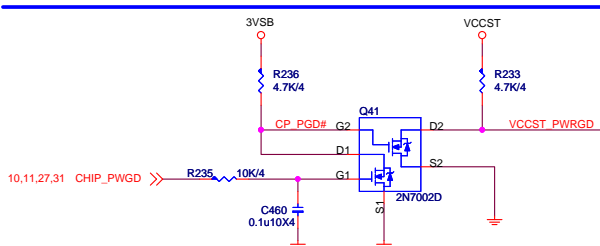
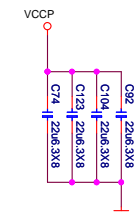


CPU SOCKET CAVITY 0805CAPS



PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

PLACE 0805CAPS Near CPU SOCKET edge

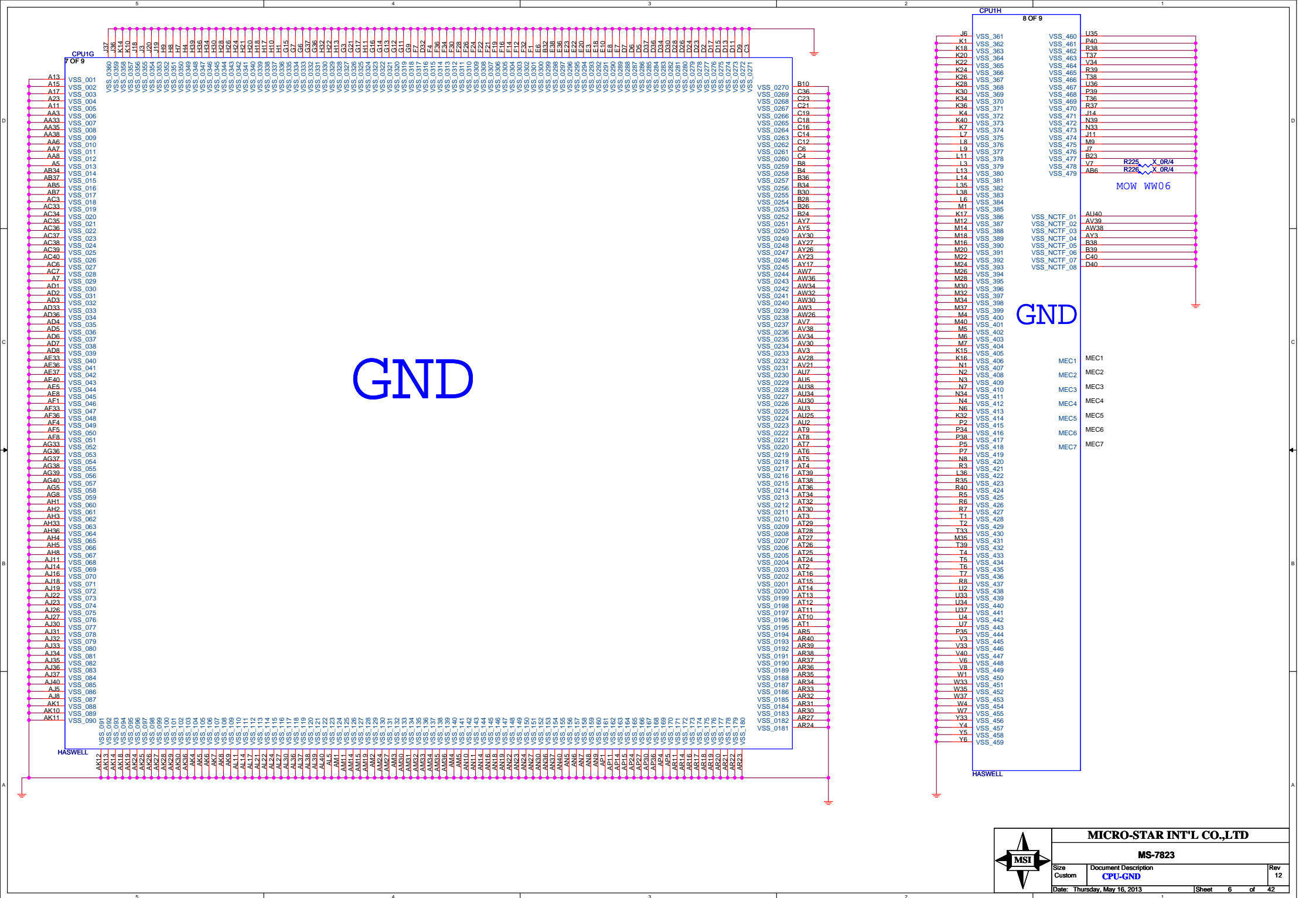


**MICRO-STAR INT'L CO.,LTD**

MS-7823

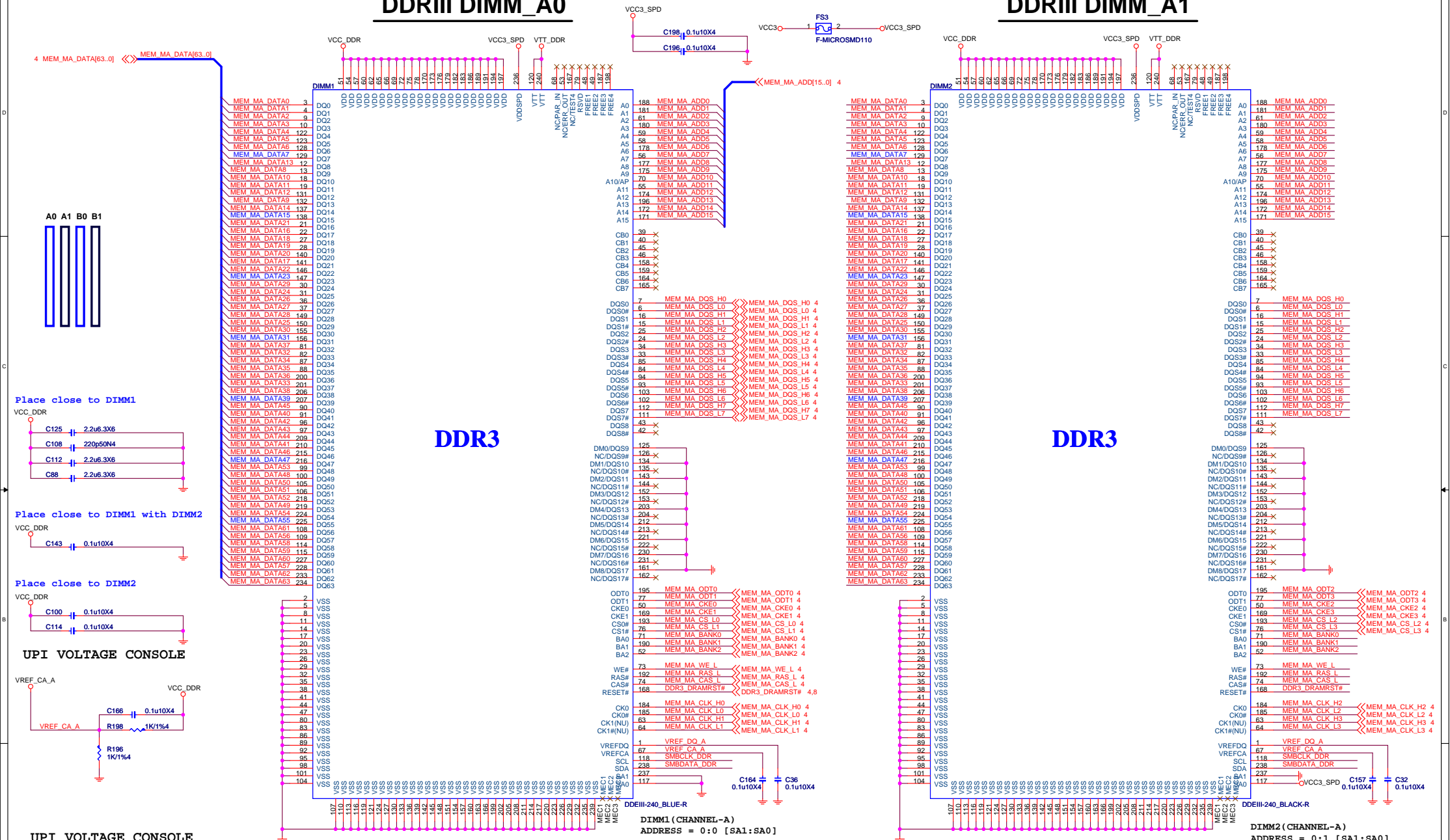
Size Custom	Document Description <b>CPU-Power</b>	Rev 12
Date: Thursday, May 16, 2013		Sheet 5 of 42





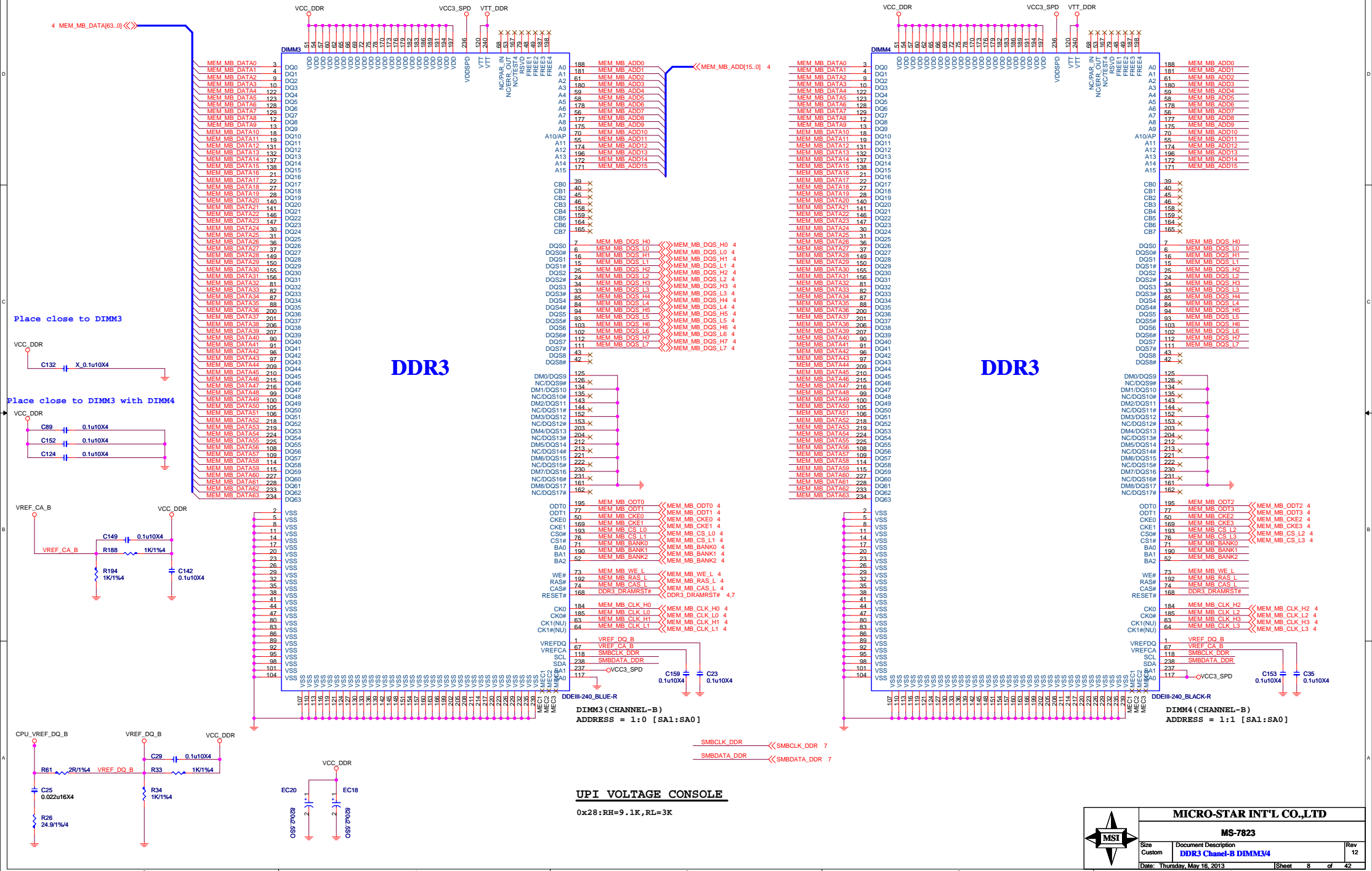
# DDRIII DIMM\_A0

# DDRIII DIMM\_A1



# DDR3 DIMM\_B0

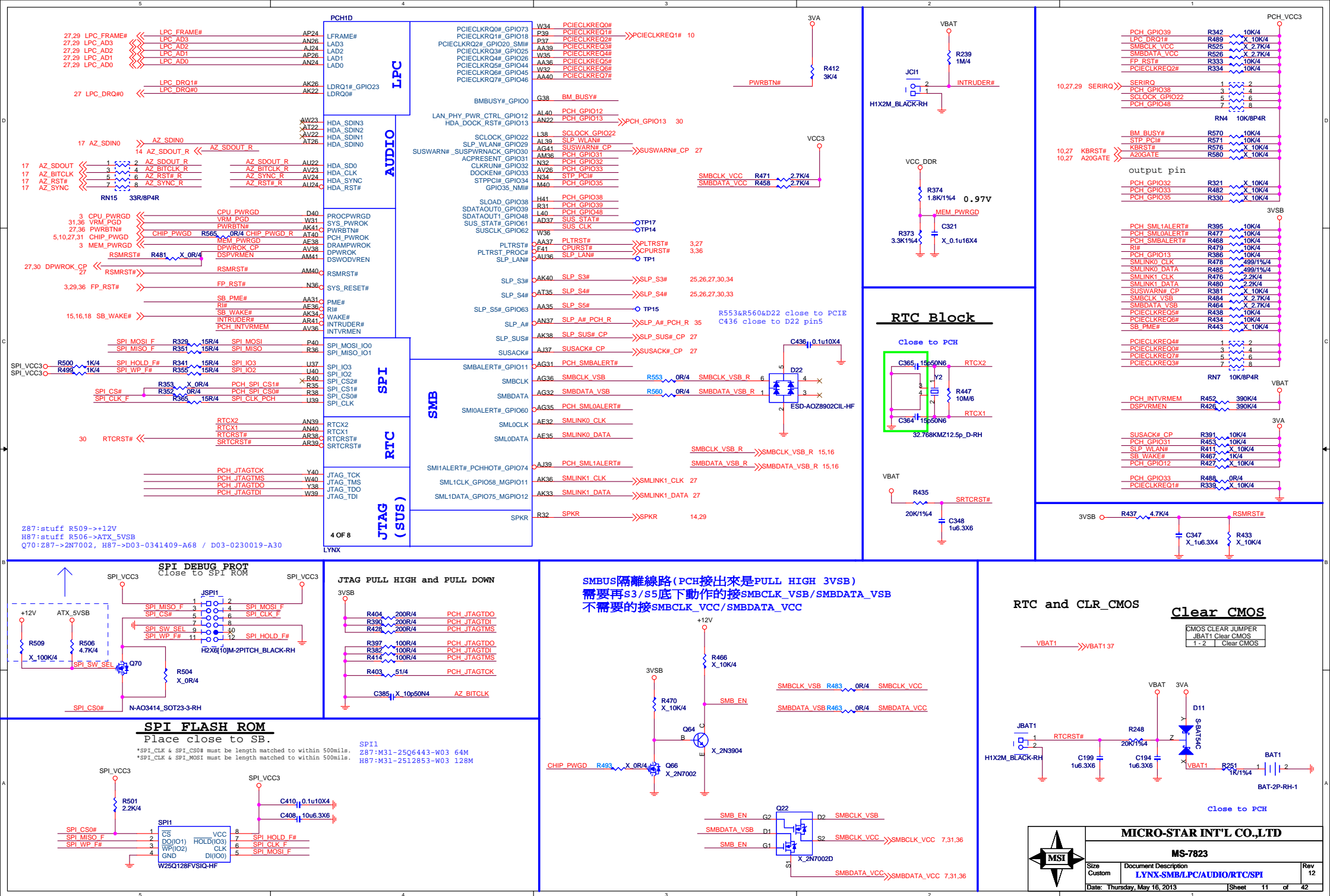
# DDR3 DIMM\_B1











AF25 ;AD25 DT CRB0.7 ASW POWER

$$(\text{Internal})\ 1.312A + (\text{External})\ 1.38A = 2.45A$$


## POWER

AG1 DT CRB0.7 VCC3 POWER

$$(\text{Internal})\ 0.261A + (\text{External})\ 0.261A = 0.522A$$

PCH VCC3 HAVE SEQCING

2013.0514.add C470

---

PCH decoupling cap

**MICRO-STAR INT'L CO.,LTD**

MS-7823

Size
------

Document Description
----------------------

Rev
-----

Date: Thursday, May 16, 2013

Sheet 12 of 42

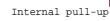
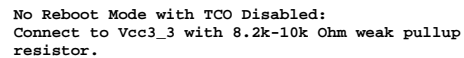
Date: T

Thursday, May 16, 2013

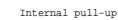
Sheet 12 of 42







Default



Top Block Swap Mode:  
Connect to ground with 4.7k Ohm weak pulldown resistor.

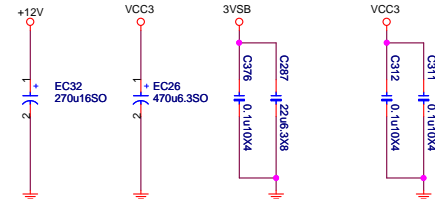
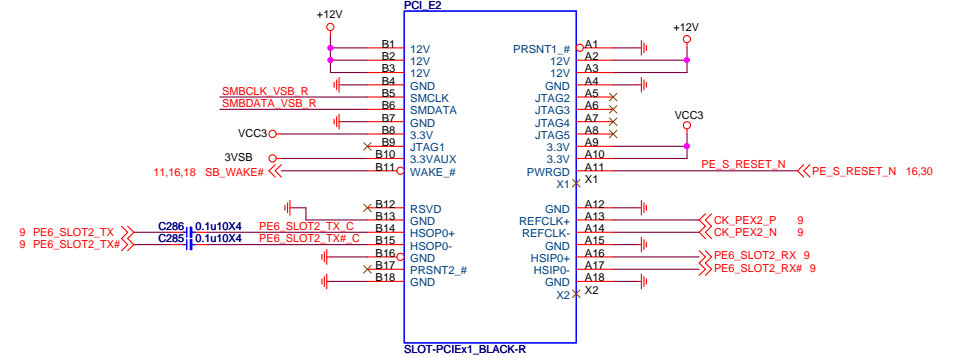


Default (Disable TLS):  
Leave NC. Internal pull down.

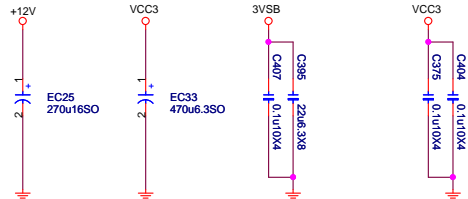
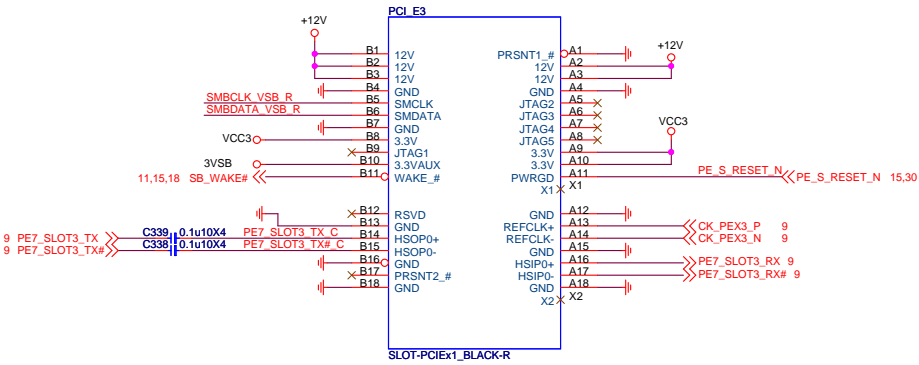


Size Custom	Document Description <b>LYNX-Strap</b>	Rev 12
Date: Thursday, May 16, 2013		Sheet 14 of 42

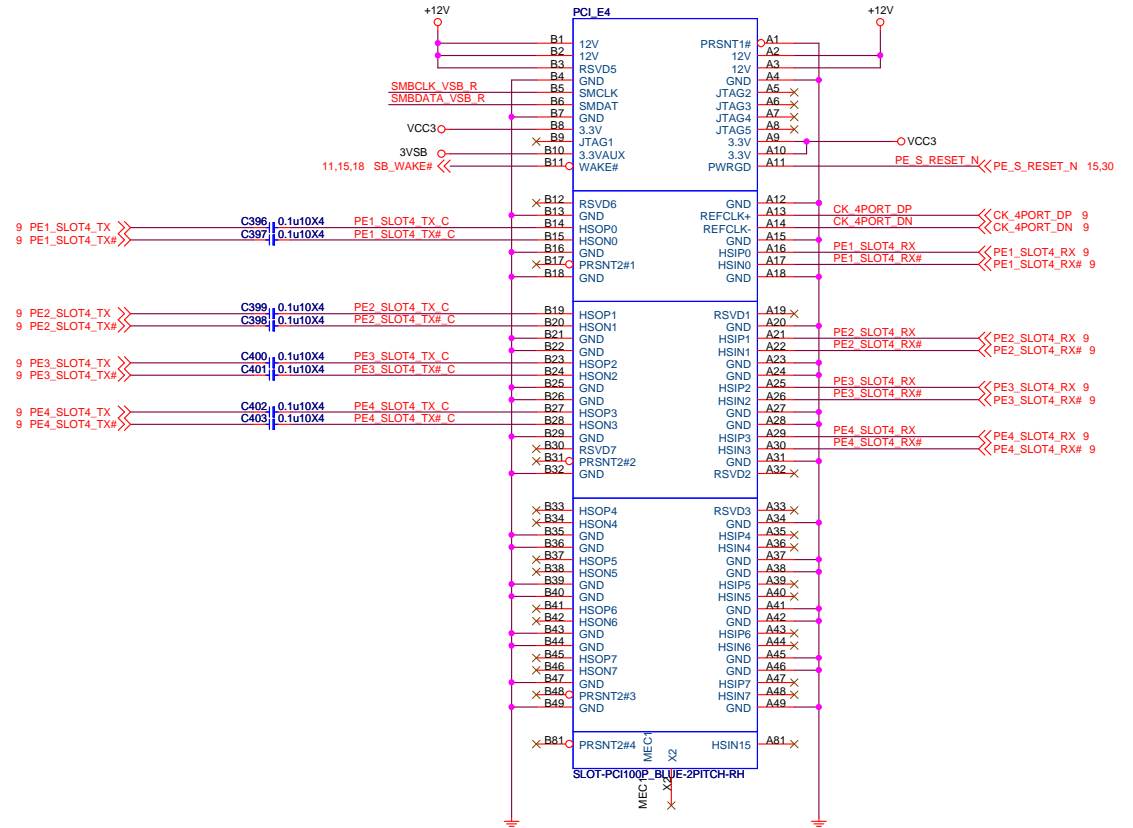
11,16 SMBCLK\_VSB\_R  
11,16 SMBDATA\_VSB\_R



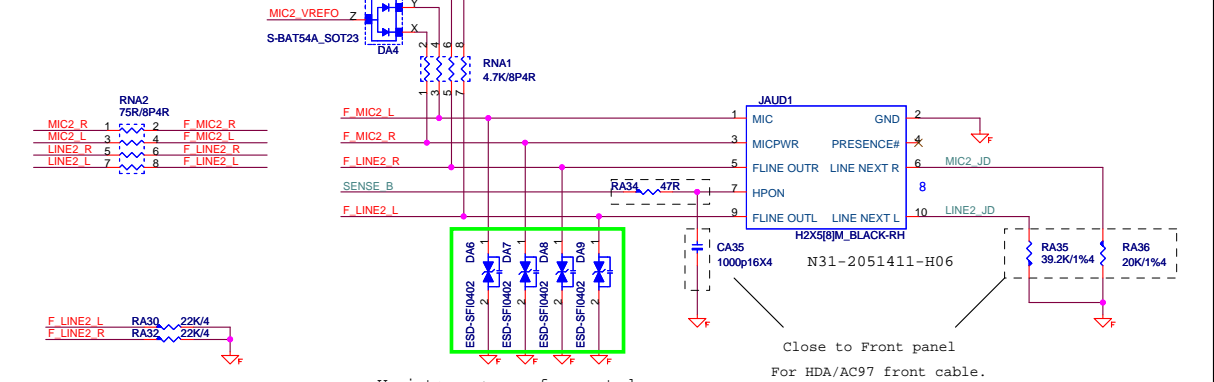
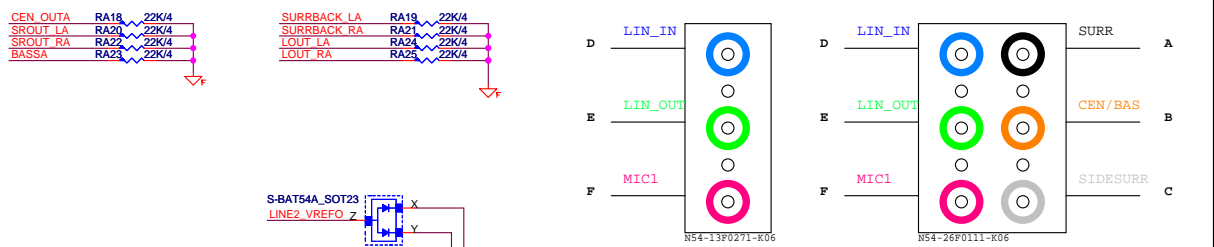
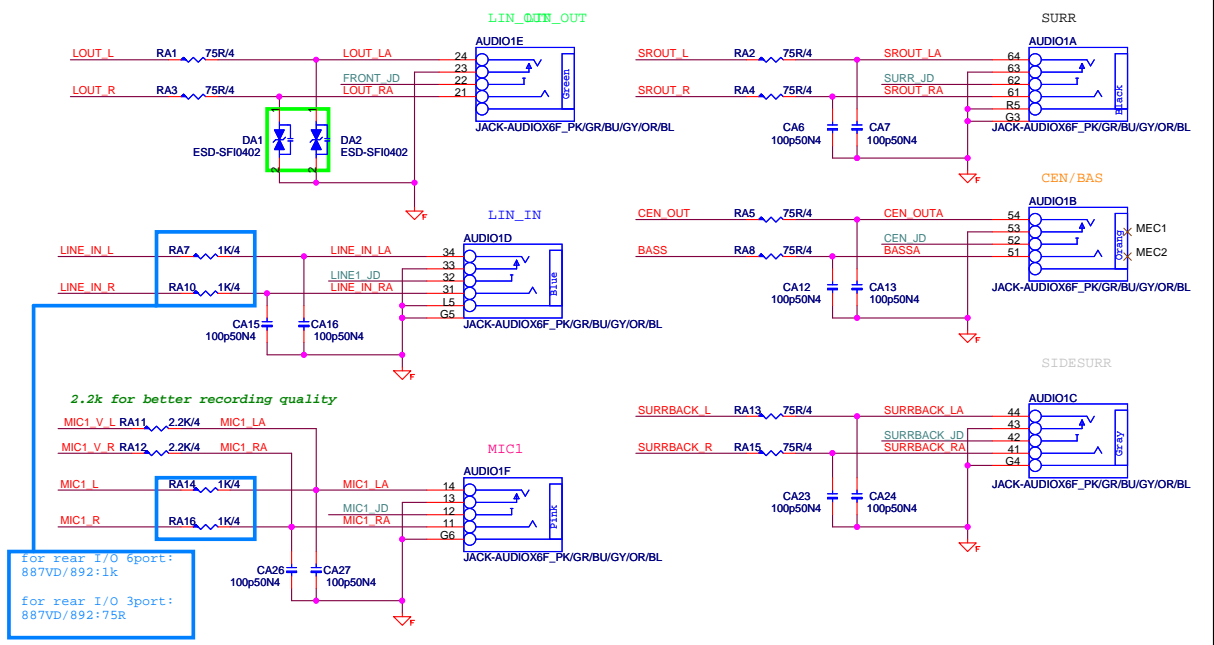
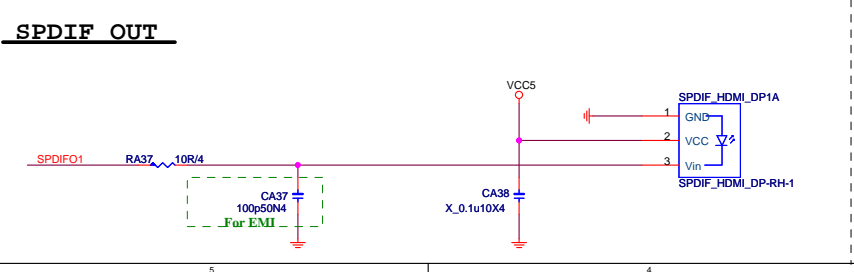
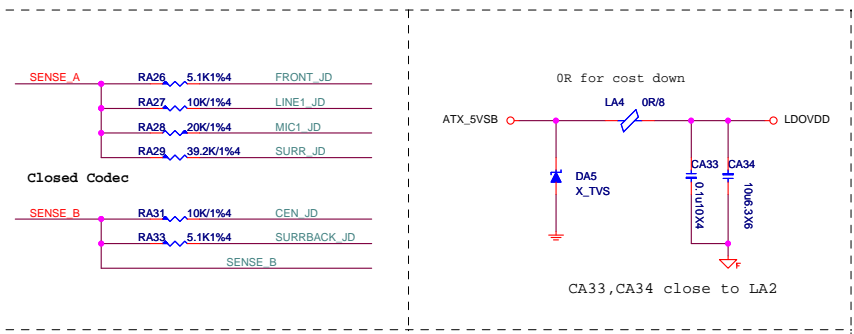
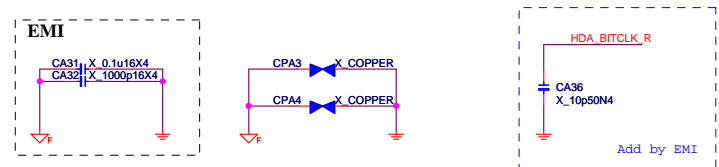
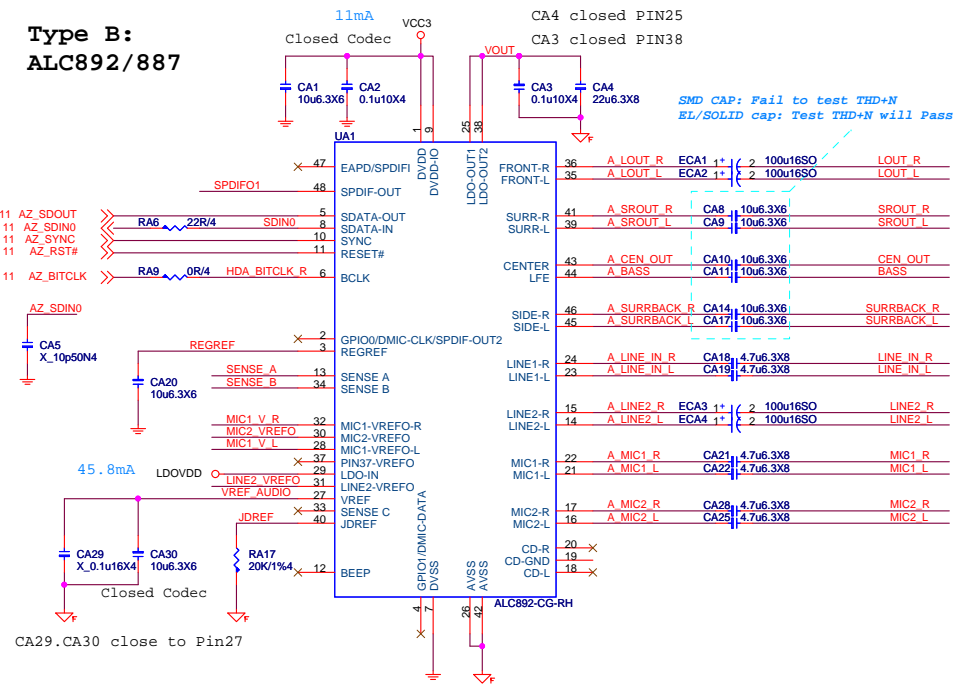
11,15 SMBCLK\_VSB\_R  
11,15 SMBDATA\_VSB\_R



## PCI Express X4 Slot



# Type B: ALC892/887



for rear I/O 6port:  
887VD/892:1k

for rear I/O 3port:  
887VD/892:75R

Close to Front panel  
For HDA/AC97 front cable.

MSI

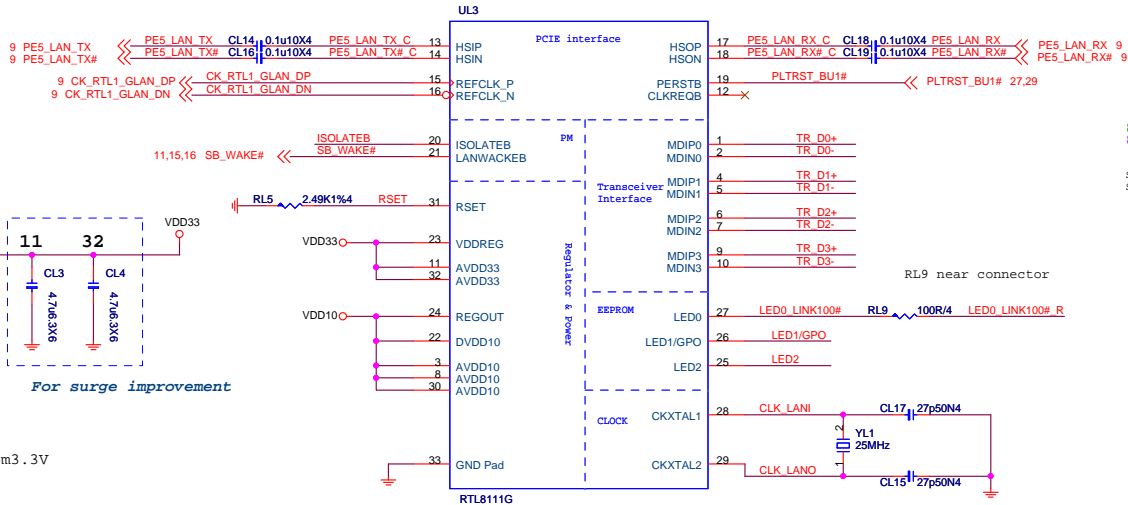
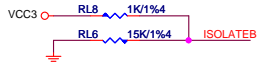
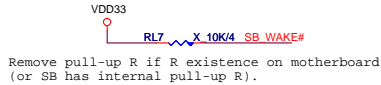
MS-7823

Size Custom Document Description

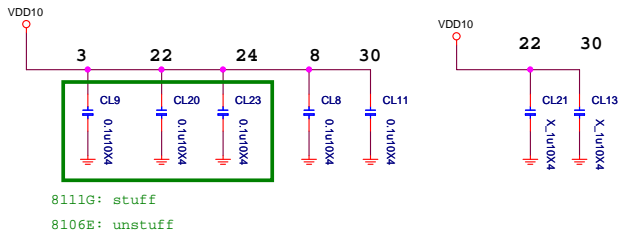
Audio Codec ALC892

Date: Thursday, May 16, 2013 Sheet 17 of 42

## RTL8106E 10/100M LAN



Pin33: 4 via from top layer to GND layer and make the via at the center of IC.



CL21 Reserve for 8111G  
CL13 reserve for 8106E

Icc10 average operating supply current from 1.0V  
At 1Gbps with heavy network traffic 300mA

```
8111G:stuff CL20,CL9,CL8,CL11,CL23
      un stuff CL13,CL21
```

```
8106E: stuff CL8,CL11,CL13
      un stuff CL21.CL20.CL9.CL23
```

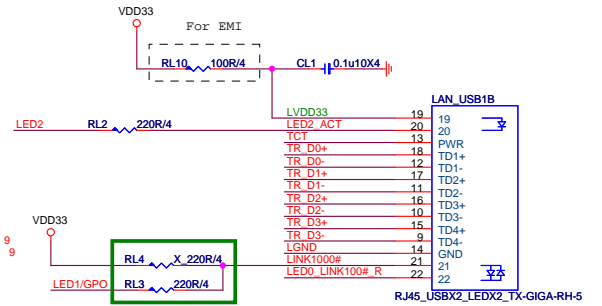
## 8106E POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	15/94	49.5/310.2
100 M Idle/TxRx	52/105	171.6/346.5
S0 ALDPS	4	13.2

## 8111G POWER Consumption

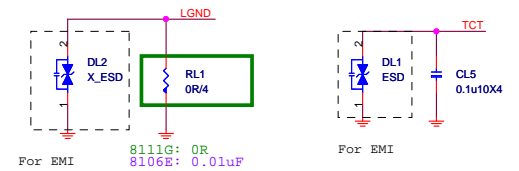
	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

### LAN Connector



8111G: Keep RL6 and Remove RL5 for RTL8111G  
8106E: Keep RL5 and Remove RL6 for RTL8106E

Support R>= 249 ohm Resister For Single Color LED.  
Support R>= 125 ohm Resister For Dual Color LED.

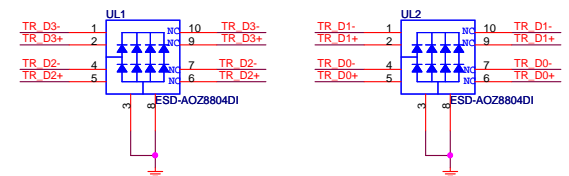


For EMI 8106E: 0.01uF

For EMI

## Reserve ESD Protect

Change to 10 pin TVS by EMI



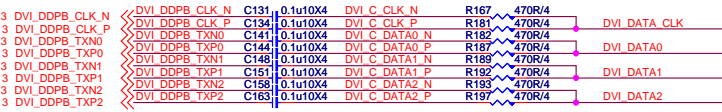
**MICRO-STAR INT'L CO.,LTD**

MS-7823

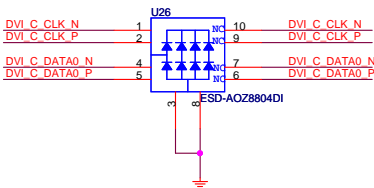
Size Custom	Document Description <b>LAN-RTL8111G</b>	Rev 12
Date: Thursday, May 16, 2013		Sheet 18 of 42



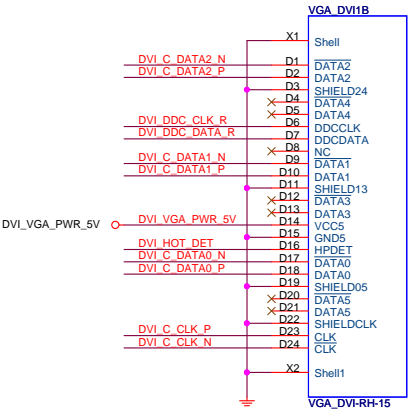
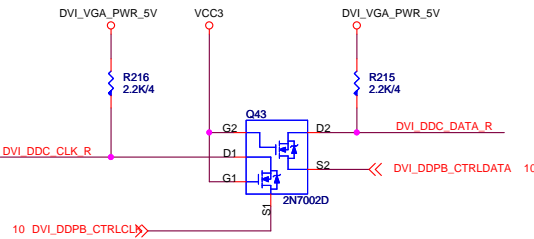
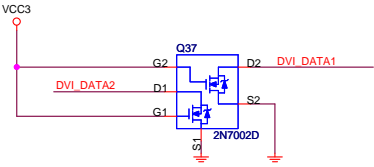
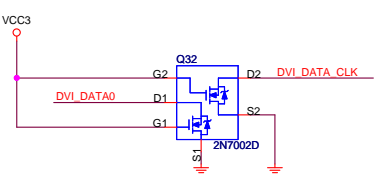
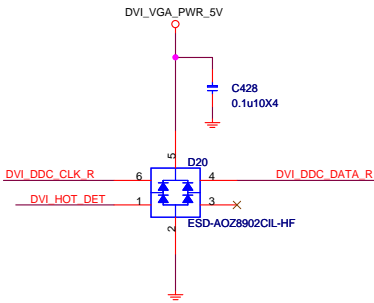
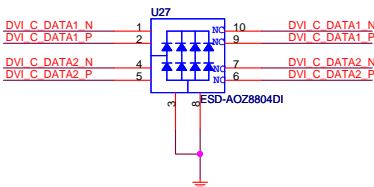
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



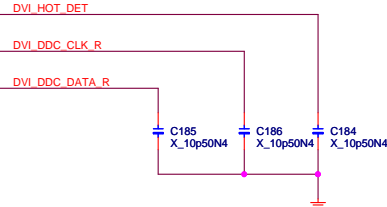
U26 AVL:D0G-05A050C-O05  
D0G-06A050C-A68



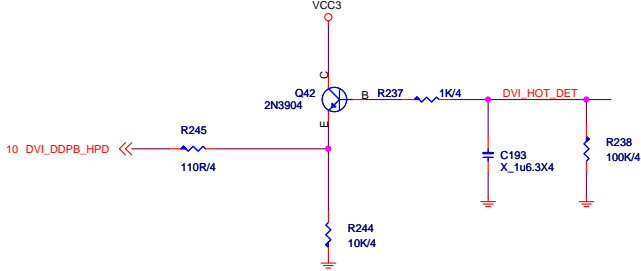
U27 AVL:D0G-05A050C-O05  
D0G-06A050C-A68



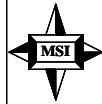
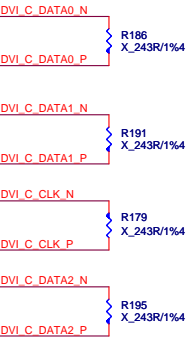
EMI



HPD



For EMI

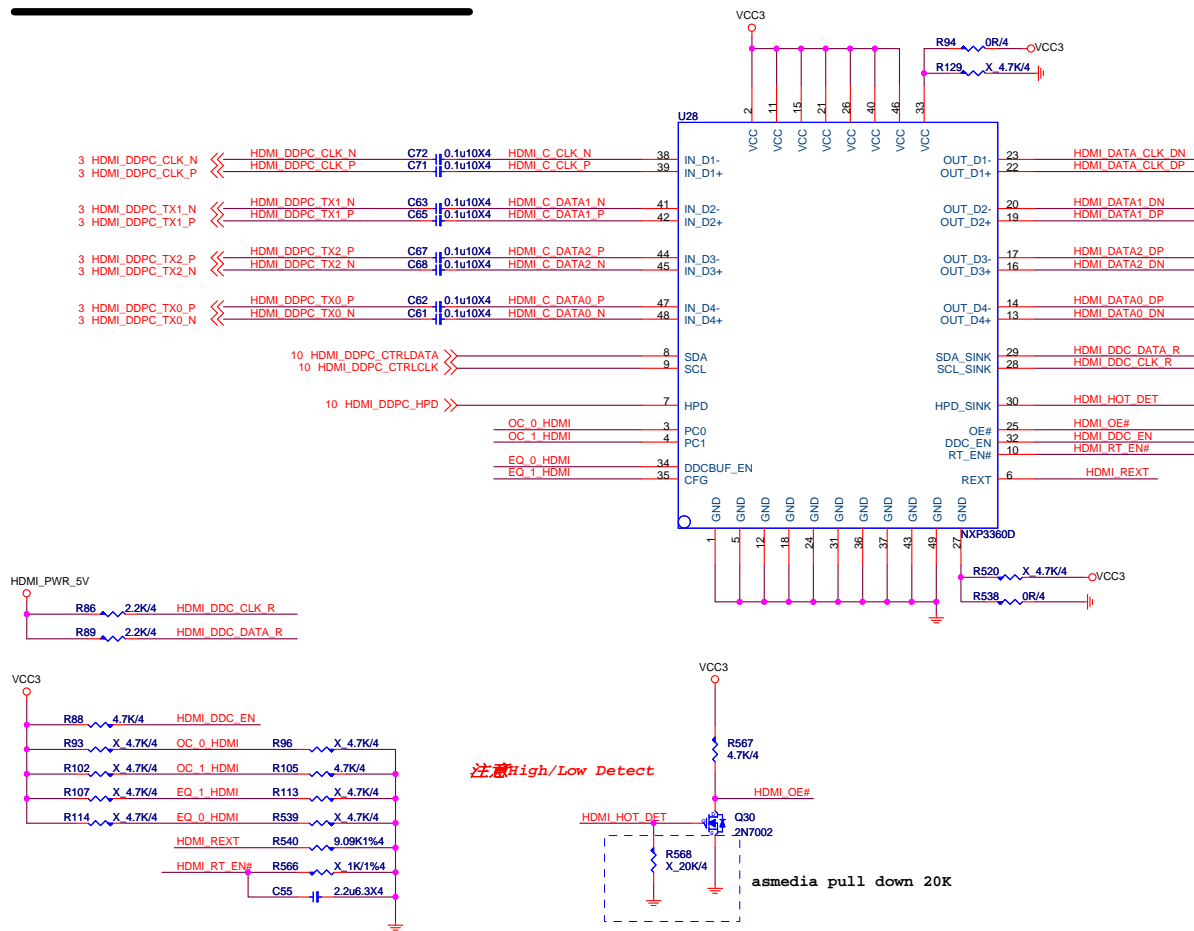


MICRO-STAR INT'L CO.,LTD

MS-7823

Size	Document Description	Rev
Custom	DVI Connector	12
Date:	Thursday, May 16, 2013	Sheet 19 of 42

# HDMI level shifter



	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

**note**

internal pull-up at ~500K ohm.

internal pull-down at ~500K ohm.

internal pull-down at ~500K ohm.

internal pull-down at ~200K ohm; 5V tolerant.

internal pull-down at ~500K ohm.

analog current generation.

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	

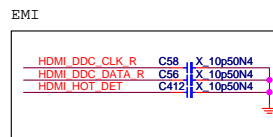
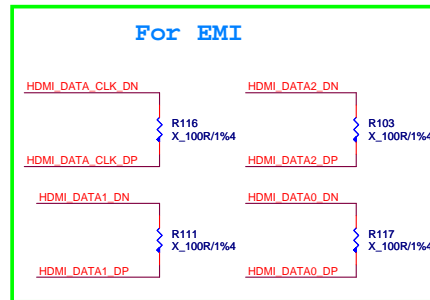
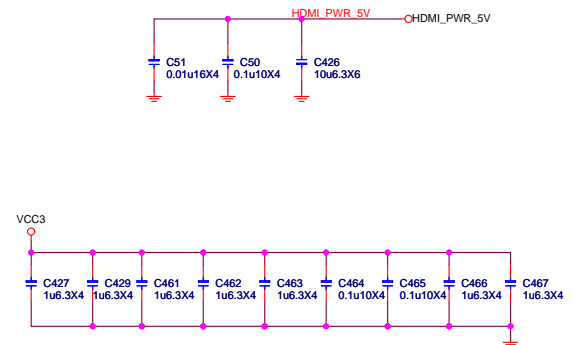
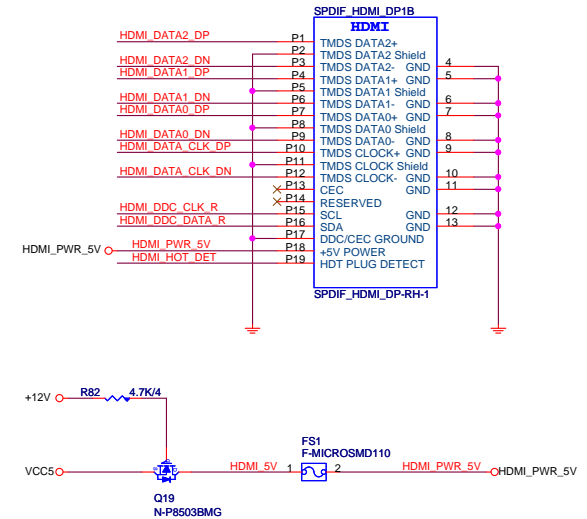


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMD5B_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMD5B_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMD5B_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMD5B_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMD5B_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMD5B_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMD5B_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMD5B_CLK	DDPB_3P
	DDPB_HPDP	DDSP_B_HPDP0	Hot plug detect used by HDMI Port B. HDMI DDC lines for Port B
	SDVO_CTRLCLK	HDMI_CTRL_CLK	
	SDVO_CTRLDATA	HDMI_CTRL_DATA	





**MICRO-STAR INT'L CO.,LTD**

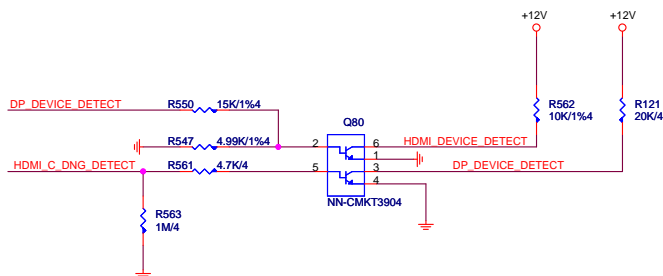
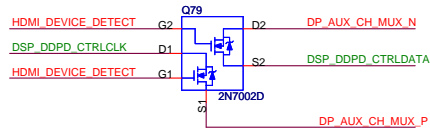
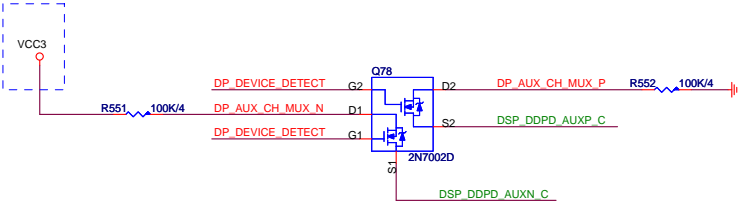
**MS-7823**

Size Custom Document Description **HDMI Connector** Rev 12

Date: Thursday, May 16, 2013 Sheet 20 of 42

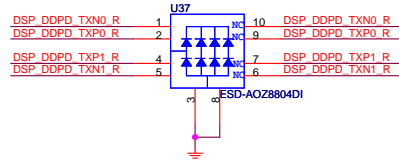
10 DSP\_DDPD\_AUXP >> DSP\_DDPD\_AUXP C458 0.1u10X4 DSP\_DDPD\_AUXP\_C  
10 DSP\_DDPD\_AUXN >> DSP\_DDPD\_AUXN C454 0.1u10X4 DSP\_DDPD\_AUXN\_C

10 DSP\_DDPD\_CTRLCLK >> DSP\_DDPD\_CTRLCLK R558 2.2K/4  
10 DSP\_DDPD\_CTRLDATA >> DSP\_DDPD\_CTRLDATA R559 2.2K/4 PCH\_VCC3

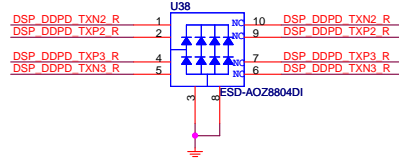


	DP	HDMI
HDMI_C_DNG_DETECT	L	H
DP_DEVICE_DETECT	H	L
HDMI_DEVICE_DETECT	L	H

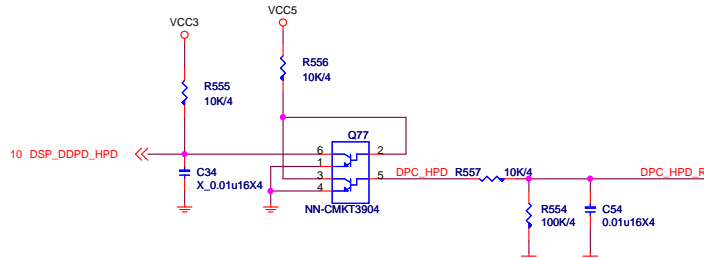
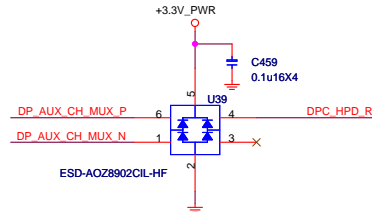
## U76 AVL:D0G-06A050C-A68



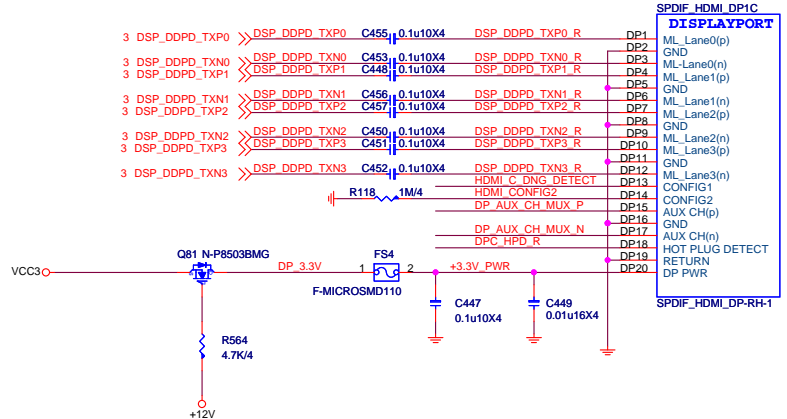
## U77 AVL:D0G-06A050C-A68



## U2 AVL:D0G-0100619-I05



## DP

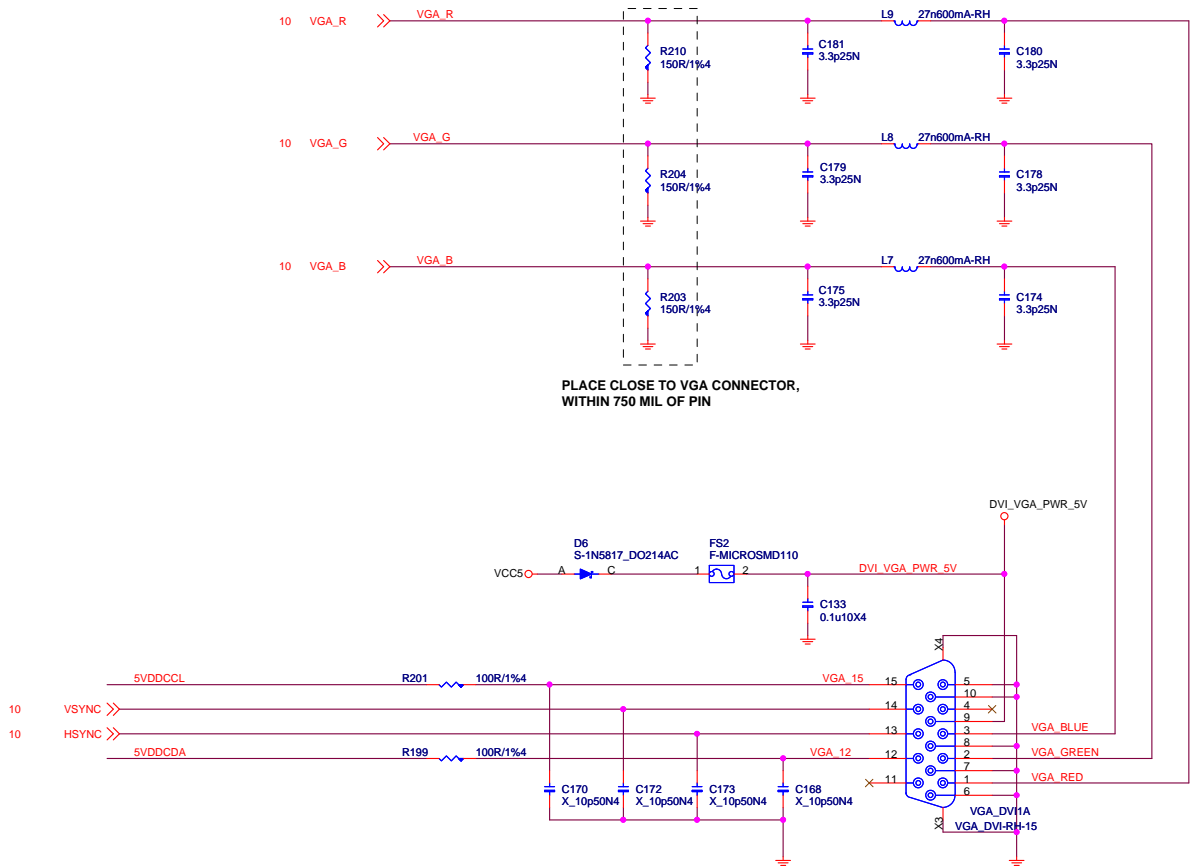
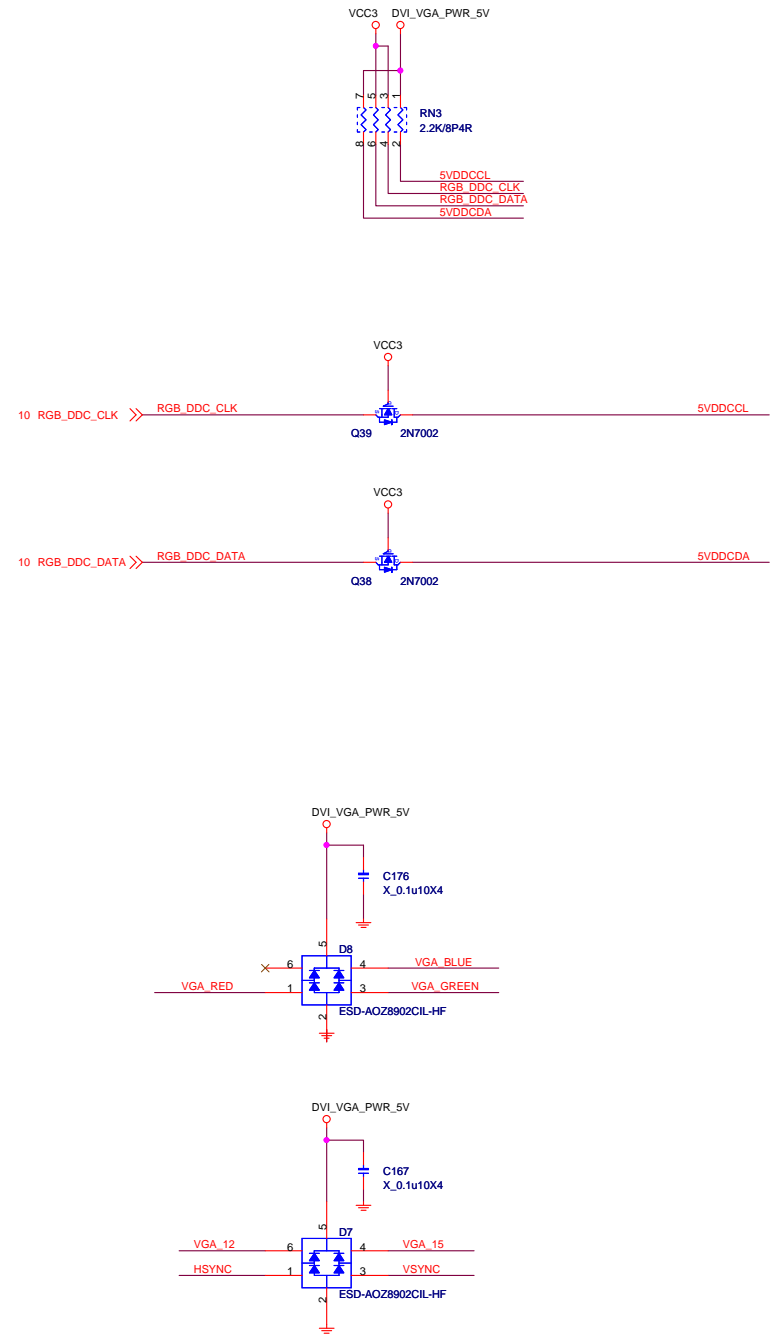


MSI			MICRO-STAR INT'L CO.,LTD		
Size			MS-7823		
Custom			Document Description		
Date: Thursday, May 16, 2013			Display port connector		
Sheet 21 of 42			Rev 12		

D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



### 3.0 Black



### 3.0 Black

Z87,H87 chip support SATA3.0  
B85 chip support SATA2.0

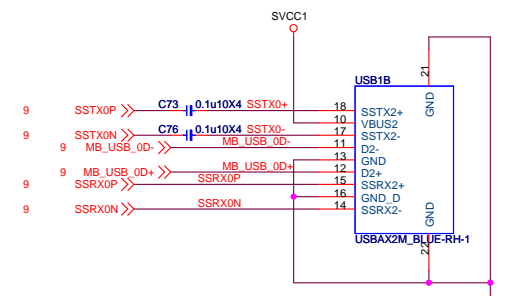
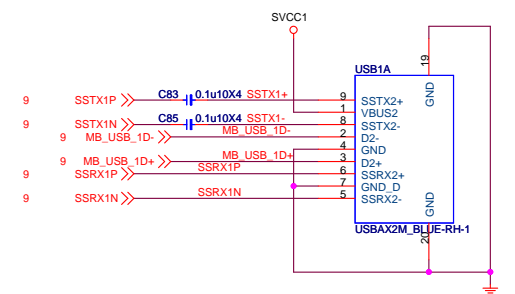
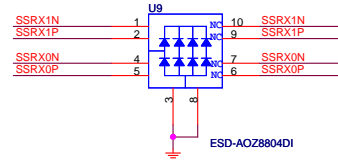
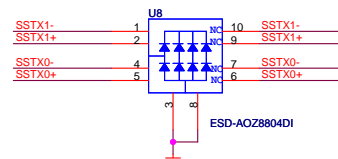
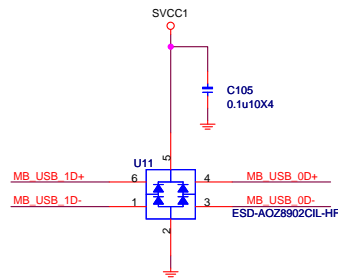
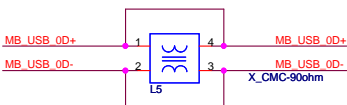
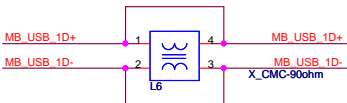
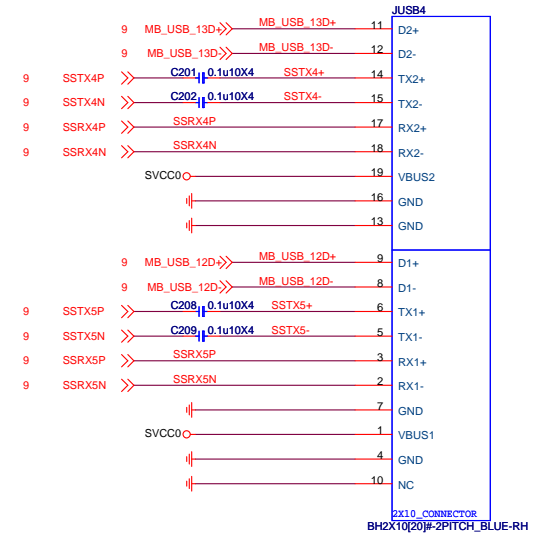
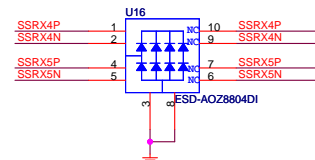
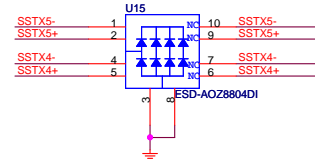
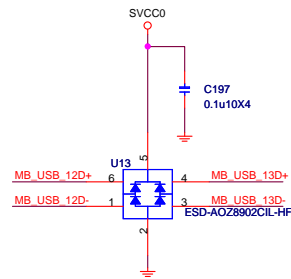
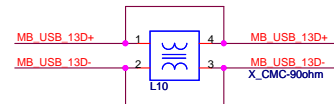
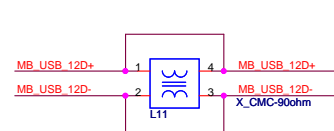


**MICRO-STAR INT'L CO.,LTD**

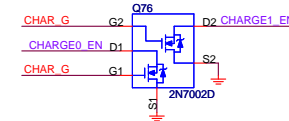
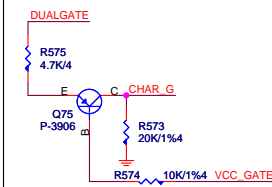
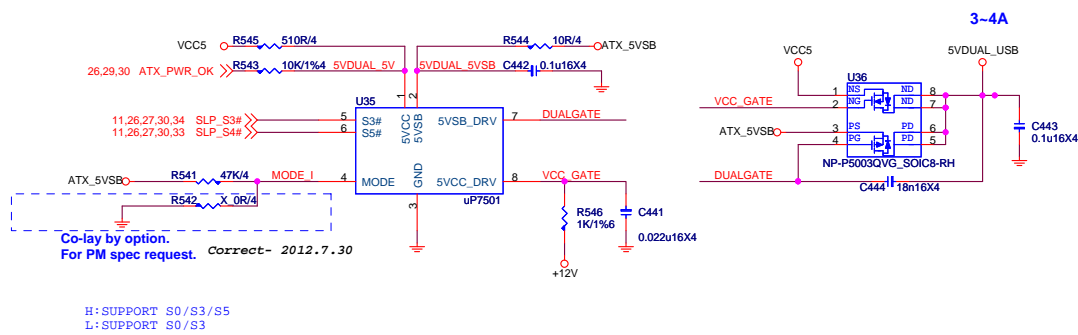
MS-7823

Size Custom	Document Description <b>SATA Connector</b>	Rev 12
Date: Thursday, May 16, 2013		Sheet 23 of 42

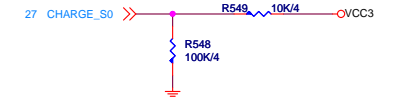




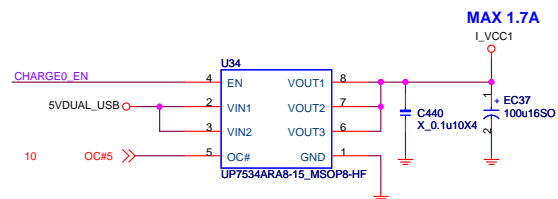
## 5VDUAL\_USB - uP7501



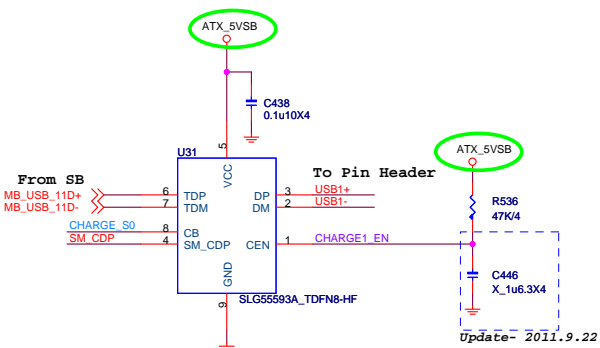
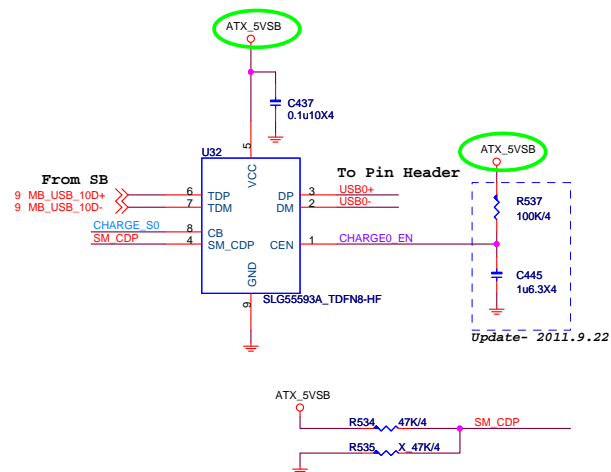
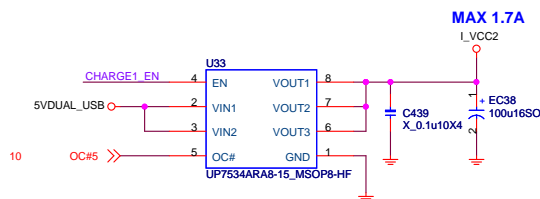
```
F71868 GPIO12
NCT6779D GPIO24
F71889 GPIO25
```



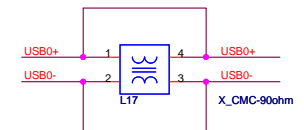
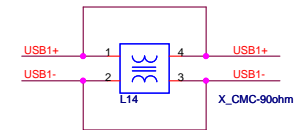
### USB POWER PORT 0 For USB Charging



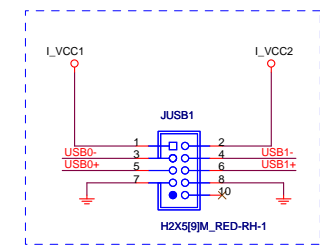
### **USB POWER PORT 1 For USB Charging**



### FRONT USB PORT 0,1



SLG55583A has internal ESD diode.



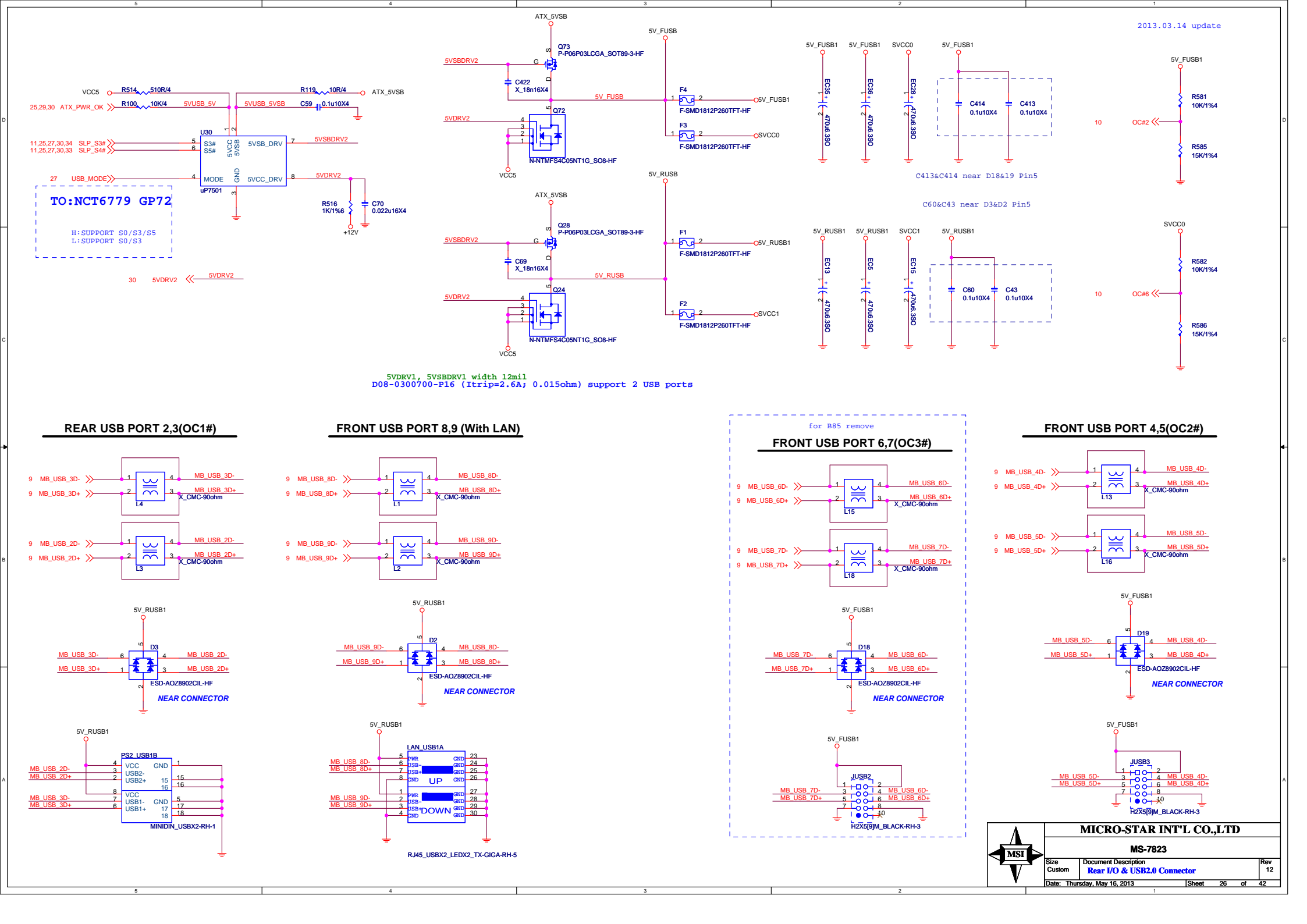
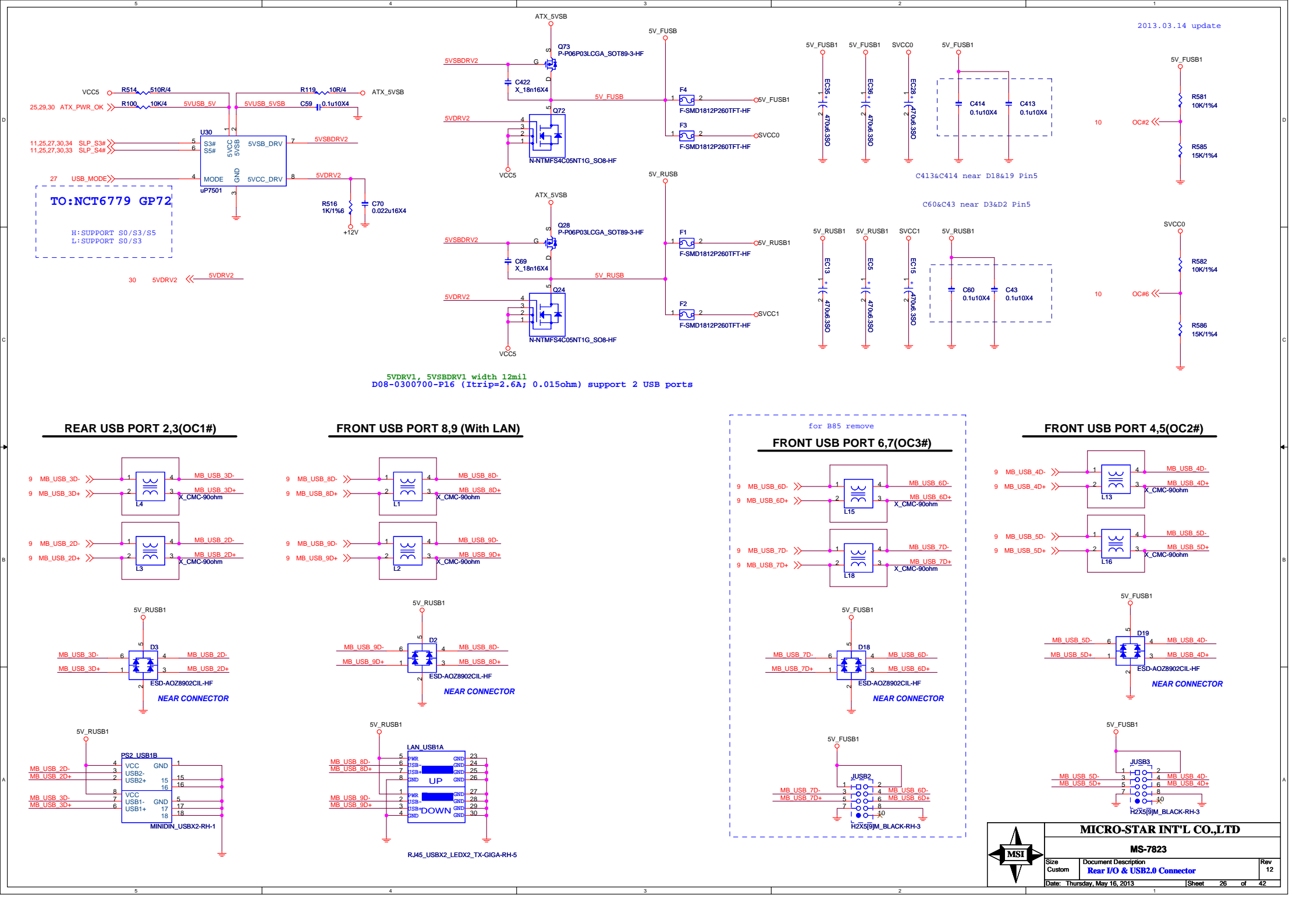
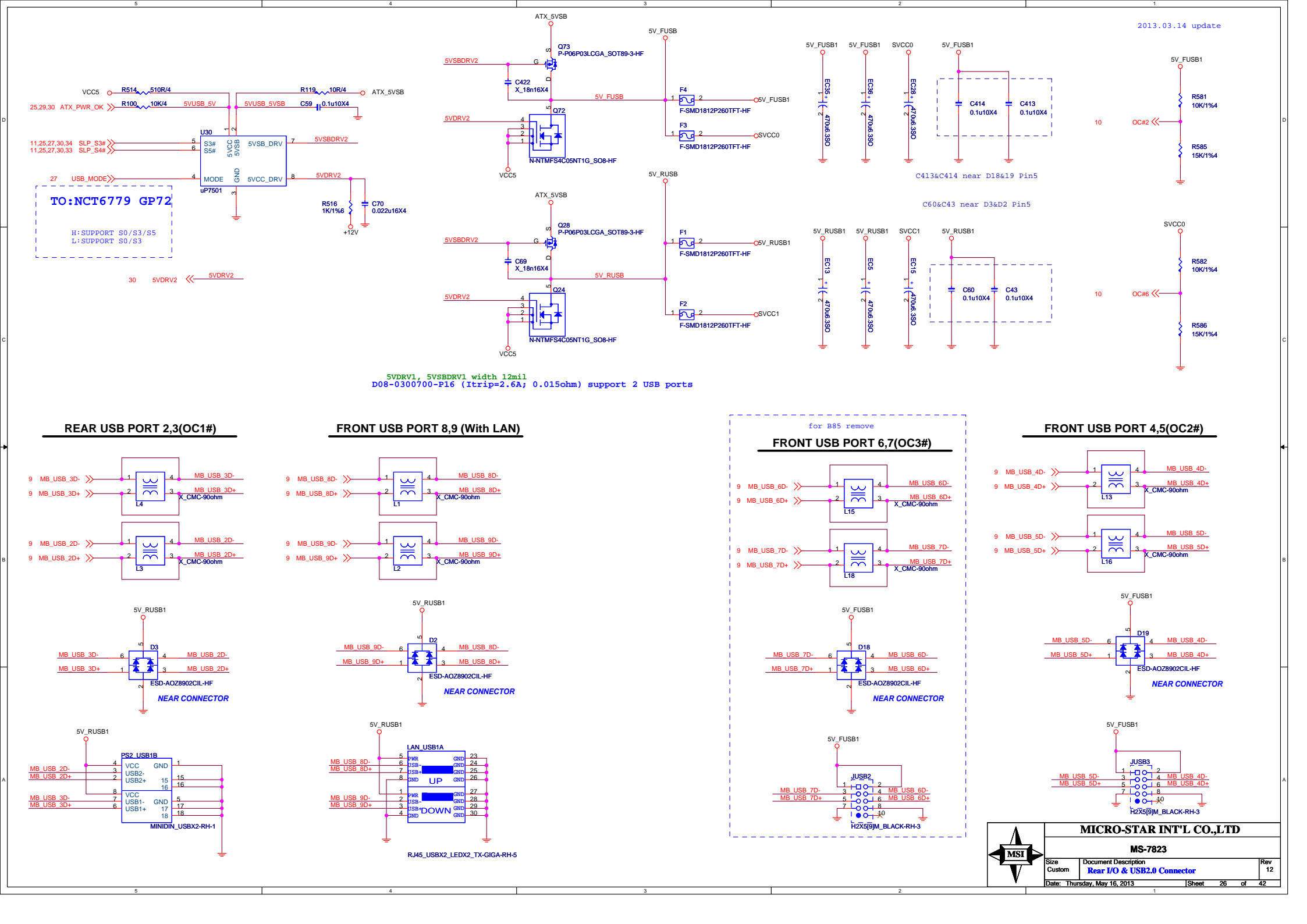
Please name the pin header JUSB1.



**MICRO-STAR INT'L CO.,LTD**

MS-7823

Size Custom	Document Description <b>25 USB CHARGE_SLG55593A</b>	Rev 12
Date: Thursday, May 16, 2013	Sheet 25 of 42	



2013.03.14 update

The diagram illustrates the internal circuitry for various USB connectors on a PCB. It includes power regulation stages for 5VUSB, 5V\_FUSB1, and 5V\_FUSB2, featuring MOSFETs (Q73, Q72, Q28, Q24), diodes (F4, F3, F1, F2), and capacitors (C422, C69, EC38, EC8, EC28, EC3, EC5, EC15, C414, C413, C60, C43). It also shows signal conditioning for USB data lines (D+, D-) using resistors (R581, R585, R582, R586) and capacitors (C413&C414, C60&C43). The layout includes detailed views of the rear USB port (2,3), front USB ports (8,9 and 4,5), and a front USB port (6,7) for B85 removal. Each port view shows the connector pinout, internal components like diodes (D3, D2, D18, D19) and capacitors (L4, L1, L15, L18, L13, L16), and the connection to the PCB pads. A note indicates a width of 12mil for 5VDRV1, 5VSBDRV1, and 5V\_FUSB1. A table at the bottom right provides the document title 'Rear I/O & USB2.0 Connector', the date 'Thursday, May 16, 2013', and the sheet number '26 of 42'.

TO:NCT6779 GP72

H: SUPPORT S0/S3/S5  
L: SUPPORT S0/S3

5VDRV1, 5VSBDRV1 width 12mil  
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 2 USB ports

REAR USB PORT 2,3(OC1#)

FRONT USB PORT 8,9 (With LAN)

FRONT USB PORT 6,7(OC3#)

FRONT USB PORT 4,5(OC2#)

MSI

MICRO-STAR INT'L CO.,LTD

MS-7823

Size Custom Document Description Rear I/O & USB2.0 Connector Rev 12

Date: Thursday, May 16, 2013 Sheet 26 of 42

2013.03.14 update

**REAR USB PORT 2,3(OC1#)**

**FRONT USB PORT 8,9 (With LAN)**

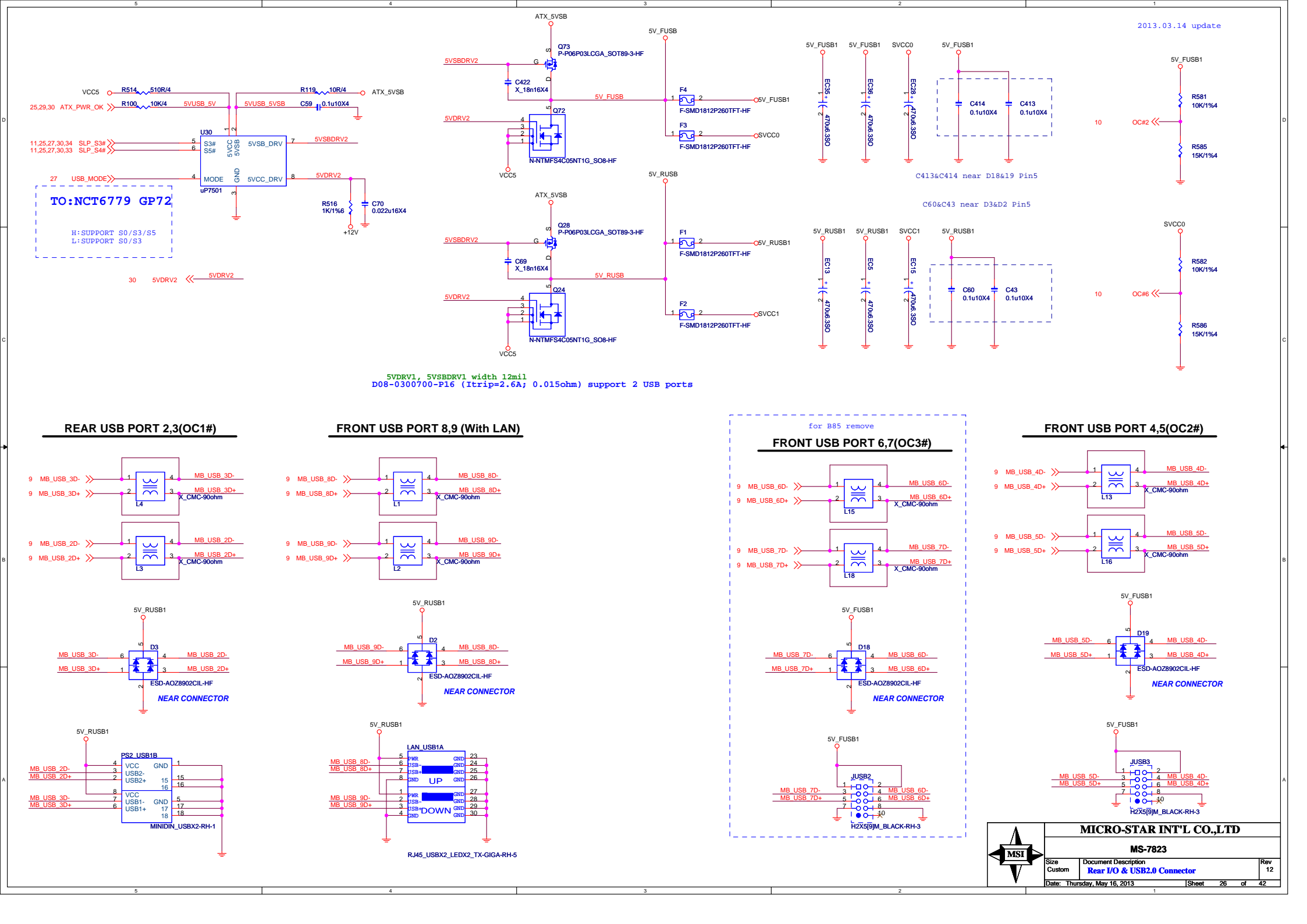
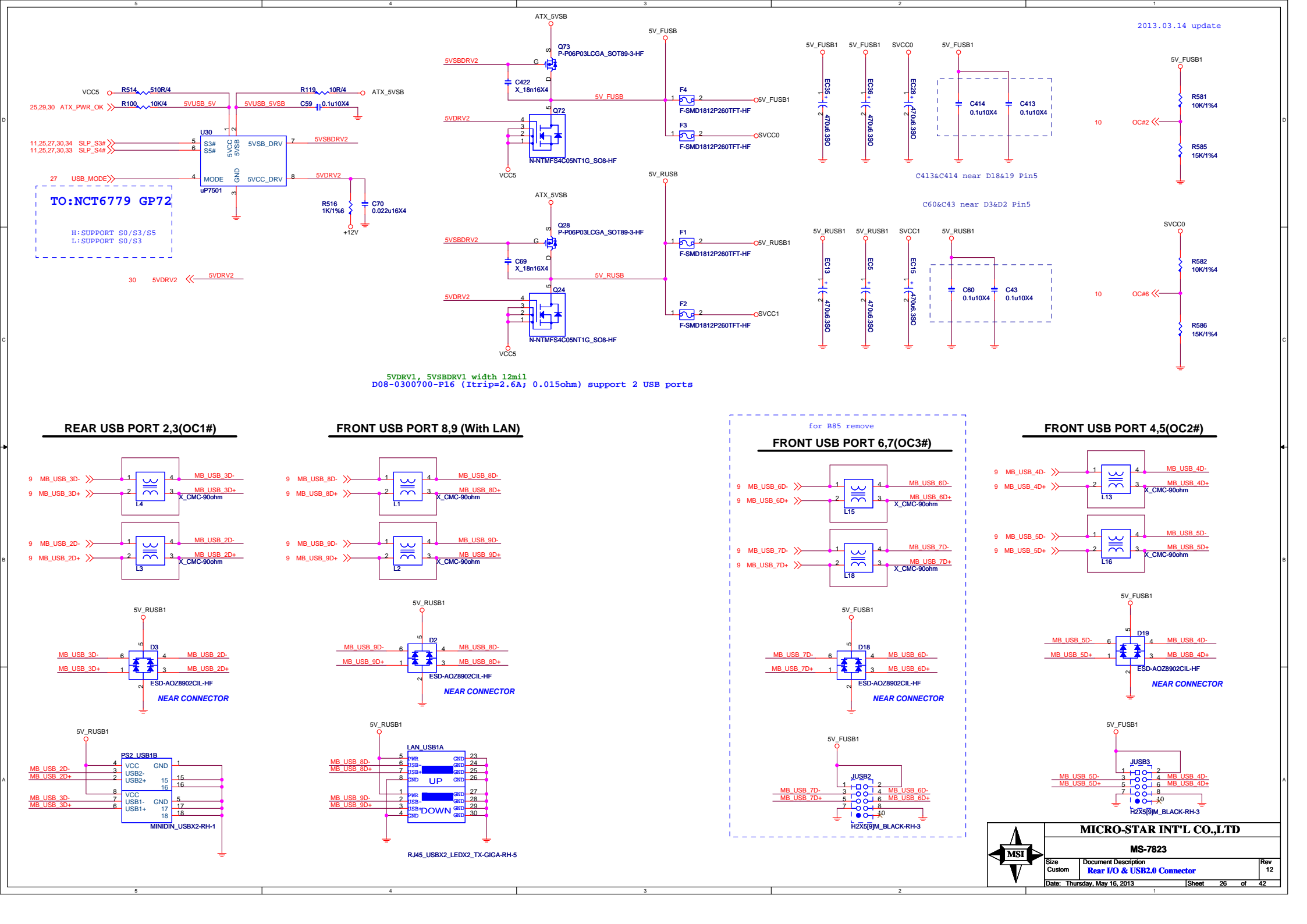
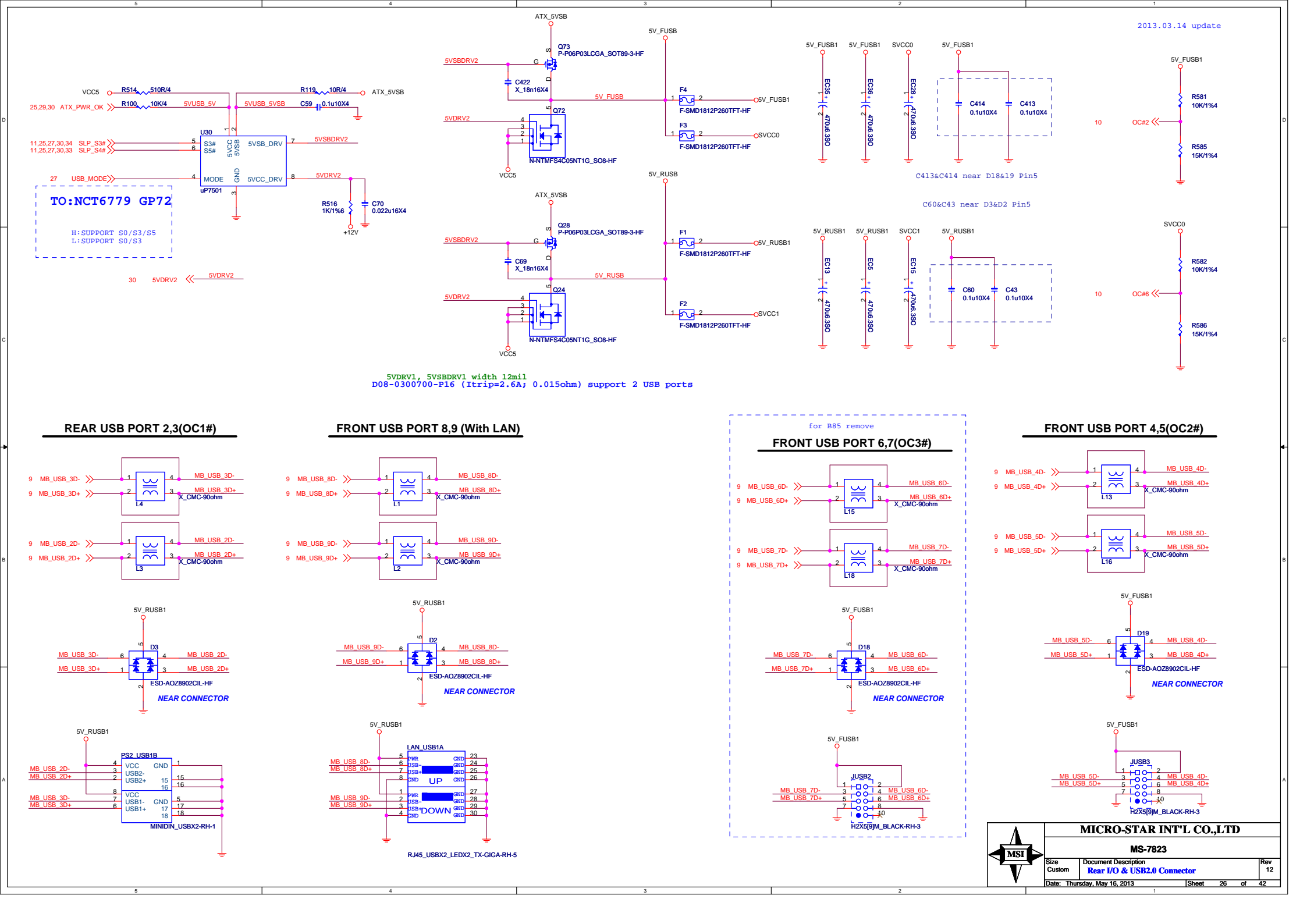
**FRONT USB PORT 6,7(OC3#)**

**FRONT USB PORT 4,5(OC2#)**

**MS-7823**

Size Custom Document Description Rear I/O & USB2.0 Connector Rev 12

Date: Thursday, May 16, 2013 Sheet 26 of 42



2013.03.14 update

The diagram illustrates the internal circuitry for various USB ports on a PCB. It includes power management sections for 5VUSB, 5V\_FUSB1, and 5V\_FUSB2, featuring MOSFETs (Q73, Q72, Q28, Q24), diodes (F4, F3, F1, F2), and capacitors (C422, C69, C413, C414, C60, C43). It also shows signal conditioning for USB signals (MB\_USB\_3D-, MB\_USB\_3D+, MB\_USB\_2D-, MB\_USB\_2D+, MB\_USB\_8D-, MB\_USB\_8D+, MB\_USB\_9D-, MB\_USB\_9D+, MB\_USB\_6D-, MB\_USB\_6D+, MB\_USB\_7D-, MB\_USB\_7D+, MB\_USB\_4D-, MB\_USB\_4D+, MB\_USB\_5D-, MB\_USB\_5D+) using components like L4, L1, L15, L18, L13, L16, D3, D2, D18, D19, and JUSB3. A note indicates 'TO:NCT6779 GP72' for support S0/S3/S5. A table at the bottom right provides document metadata.

**REAR USB PORT 2,3(OC1#)**

**FRONT USB PORT 8,9 (With LAN)**

**FRONT USB PORT 6,7(OC3#)**

**FRONT USB PORT 4,5(OC2#)**

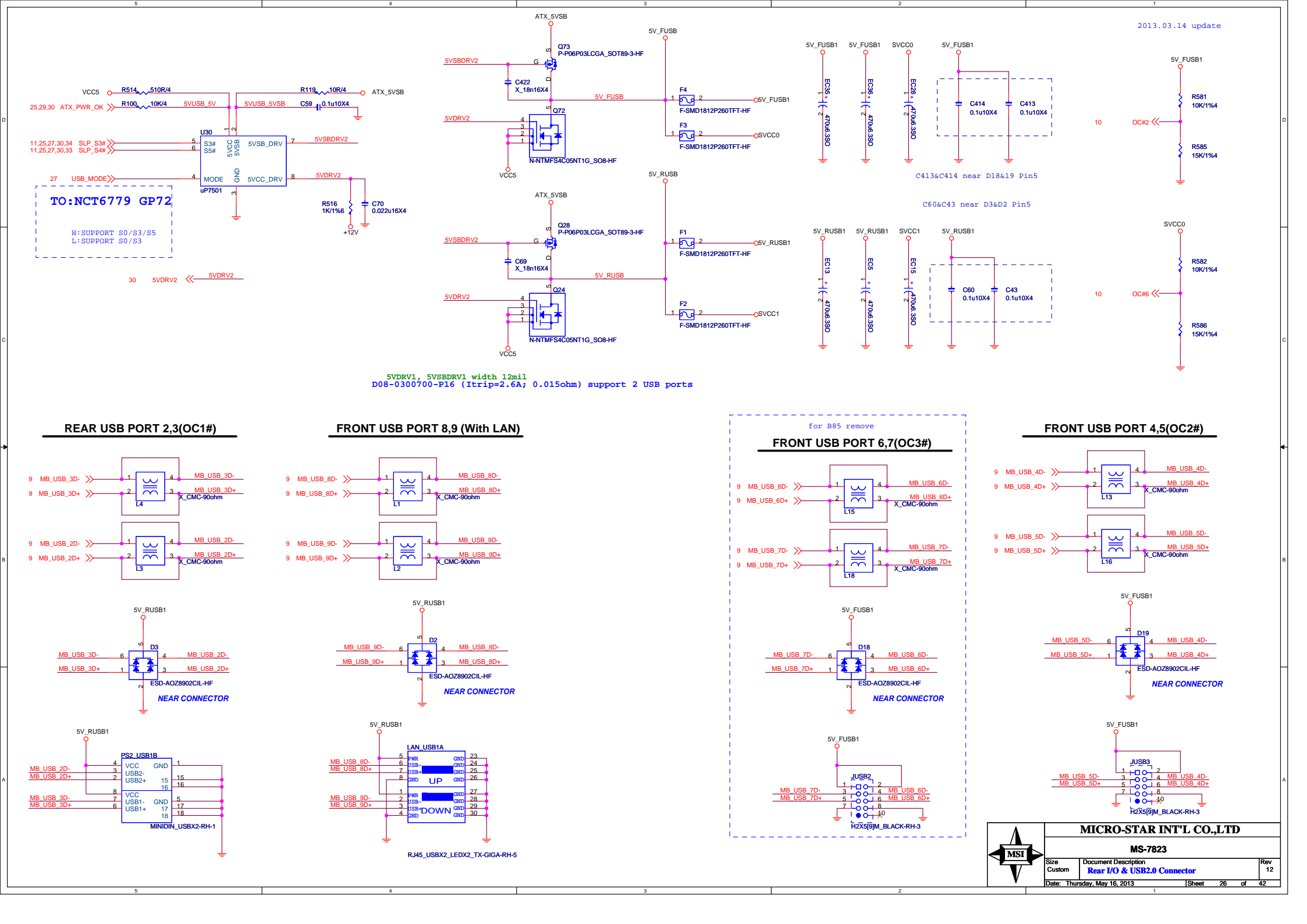
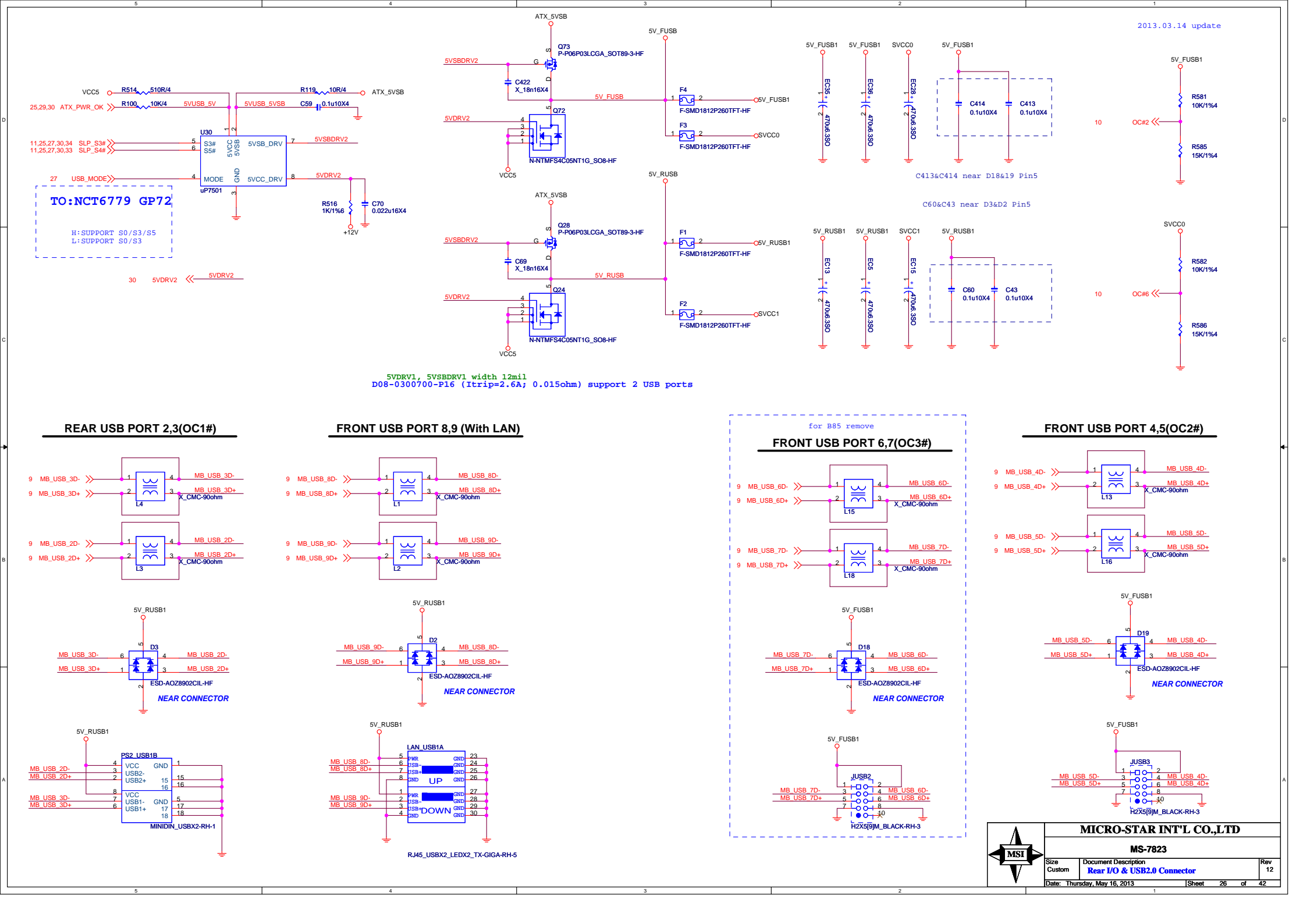
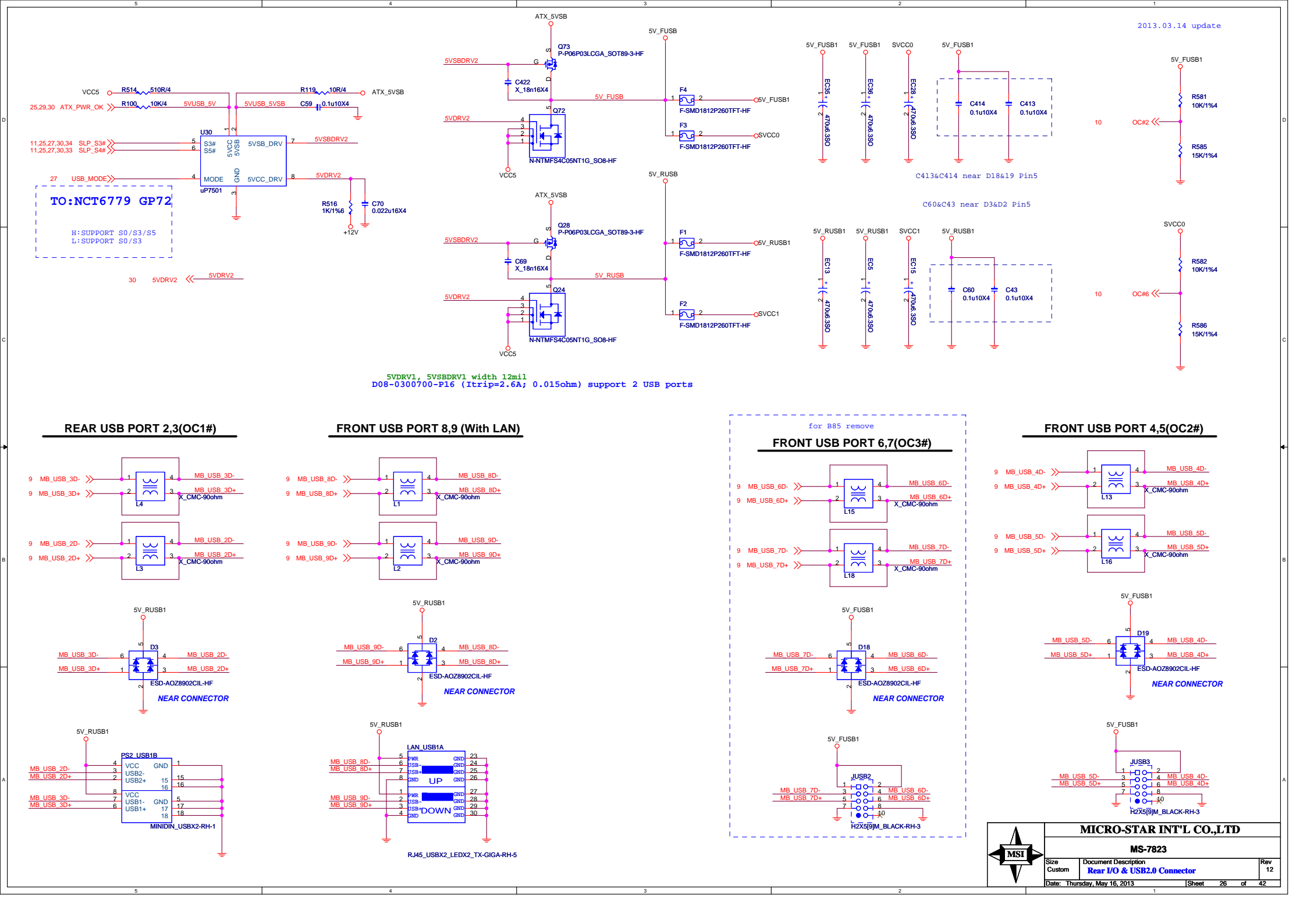
MSI

**MICRO-STAR INT'L CO.,LTD**

**MS-7823**

Size	Document Description	Rev
Custom	Rear I/O & USB2.0 Connector	12

Date: Thursday, May 16, 2013 Sheet 26 of 42



2013.03.14 update

The diagram illustrates the internal circuitry for various USB ports on a PCB. It includes power management sections for 5VUSB, 5V\_FUSB1, and 5V\_FUSB2, featuring MOSFETs (Q73, Q72, Q28, Q24), diodes (F4, F3, F1, F2), and capacitors (C422, C69, C413, C414, C60, C43). It also shows signal conditioning for USB signals (MB\_USB\_3D-, MB\_USB\_3D+, MB\_USB\_2D-, MB\_USB\_2D+, MB\_USB\_8D-, MB\_USB\_8D+, MB\_USB\_9D-, MB\_USB\_9D+, MB\_USB\_6D-, MB\_USB\_6D+, MB\_USB\_7D-, MB\_USB\_7D+, MB\_USB\_4D-, MB\_USB\_4D+, MB\_USB\_5D-, MB\_USB\_5D+) using components like L4, L1, L15, L18, L13, L16, D3, D2, D18, D19, and JUSB3. A note indicates 'TO:NCT6779 GP72' for support S0/S3/S5 and S0/S3. A warning 'H: SUPPORT S0/S3/S5 L: SUPPORT S0/S3' is present. A note '5VDRV1, 5VSBDRV1 width 12mil D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 2 USB ports' is included. A note 'for B85 remove' is present near the FRONT USB PORT 6,7(OC3#) section. A note 'R45\_USB2\_LED2\_TX-GIGA-RH-5' is present near the LAN\_USB1A section. A note 'H2X59JM\_BLACK-RH-3' is present near the JUSB3 section. A note 'R581 10K/1%4' and 'R585 15K/1%4' are present near the 5V\_FUSB1 section. A note 'R582 10K/1%4' and 'R586 15K/1%4' are present near the 5V\_FUSB2 section. A note 'OC#2' and 'OC#6' are present near the 5V\_FUSB1 and 5V\_FUSB2 sections respectively. A note 'C60&C43 near D3&D2 Pin5' is present near the 5V\_FUSB1 section. A note 'C413&C414 near D18&19 Pin5' is present near the 5V\_FUSB2 section. A note 'R581 10K/1%4' and 'R585 15K/1%4' are present near the 5V\_FUSB1 section. A note 'R582 10K/1%4' and 'R586 15K/1%4' are present near the 5V\_FUSB2 section. A note 'OC#2' and 'OC#6' are present near the 5V\_FUSB1 and 5V\_FUSB2 sections respectively. A note 'C60&C43 near D3&D2 Pin5' is present near the 5V\_FUSB1 section. A note 'C413&C414 near D18&19 Pin5' is present near the 5V\_FUSB2 section.

**REAR USB PORT 2,3(OC1#)**

**FRONT USB PORT 8,9 (With LAN)**

**FRONT USB PORT 6,7(OC3#)**

**FRONT USB PORT 4,5(OC2#)**

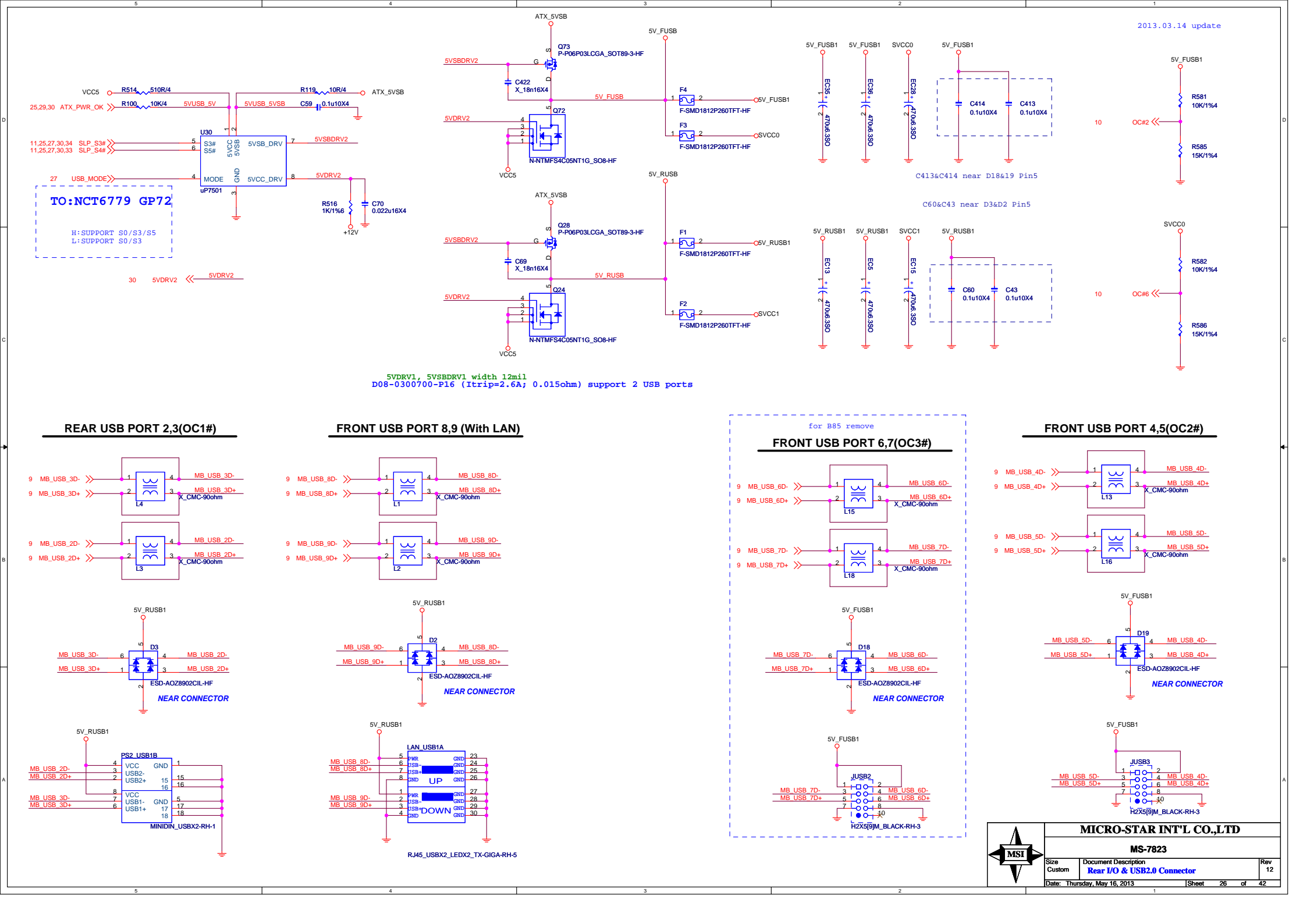
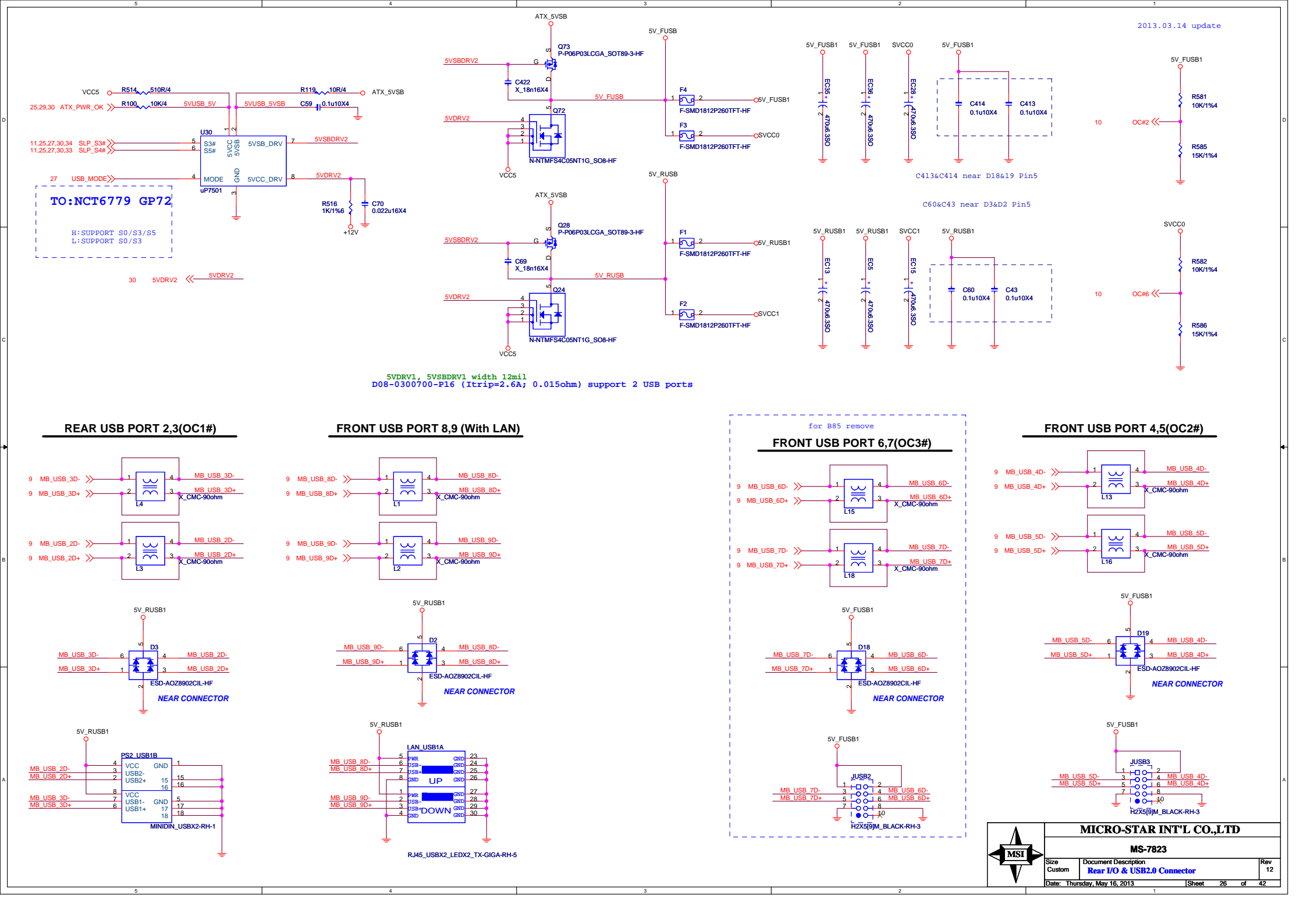
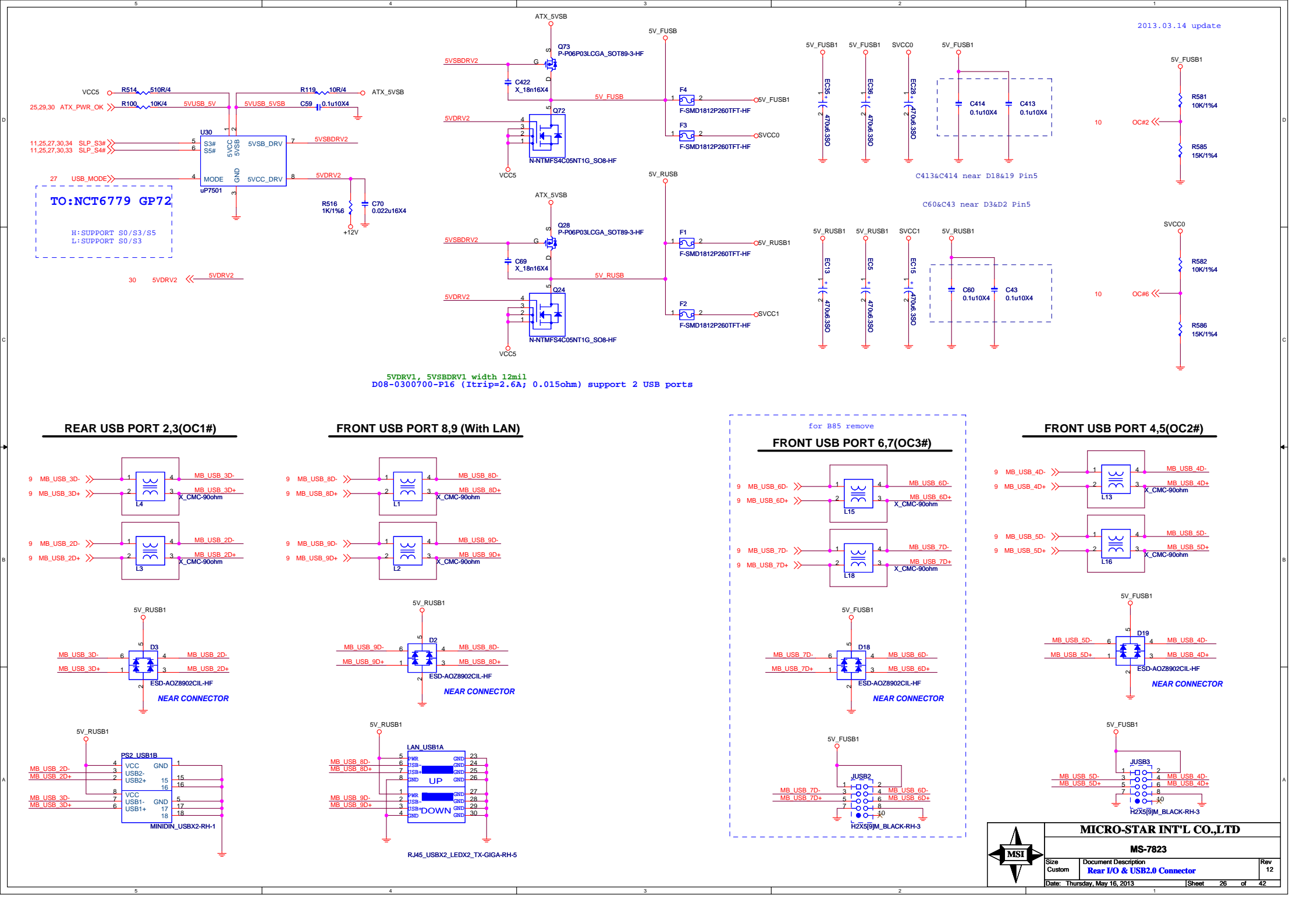
**MSI**

**MICRO-STAR INT'L CO.,LTD**

**MS-7823**

Size Custom Document Description **Rear I/O & USB2.0 Connector** Rev 12

Date: Thursday, May 16, 2013 Sheet 26 of 42



2013.03.14 update

**REAR USB PORT 2,3(OC1#)**

**FRONT USB PORT 8,9 (With LAN)**

**FRONT USB PORT 6,7(OC3#)**

**FRONT USB PORT 4,5(OC2#)**

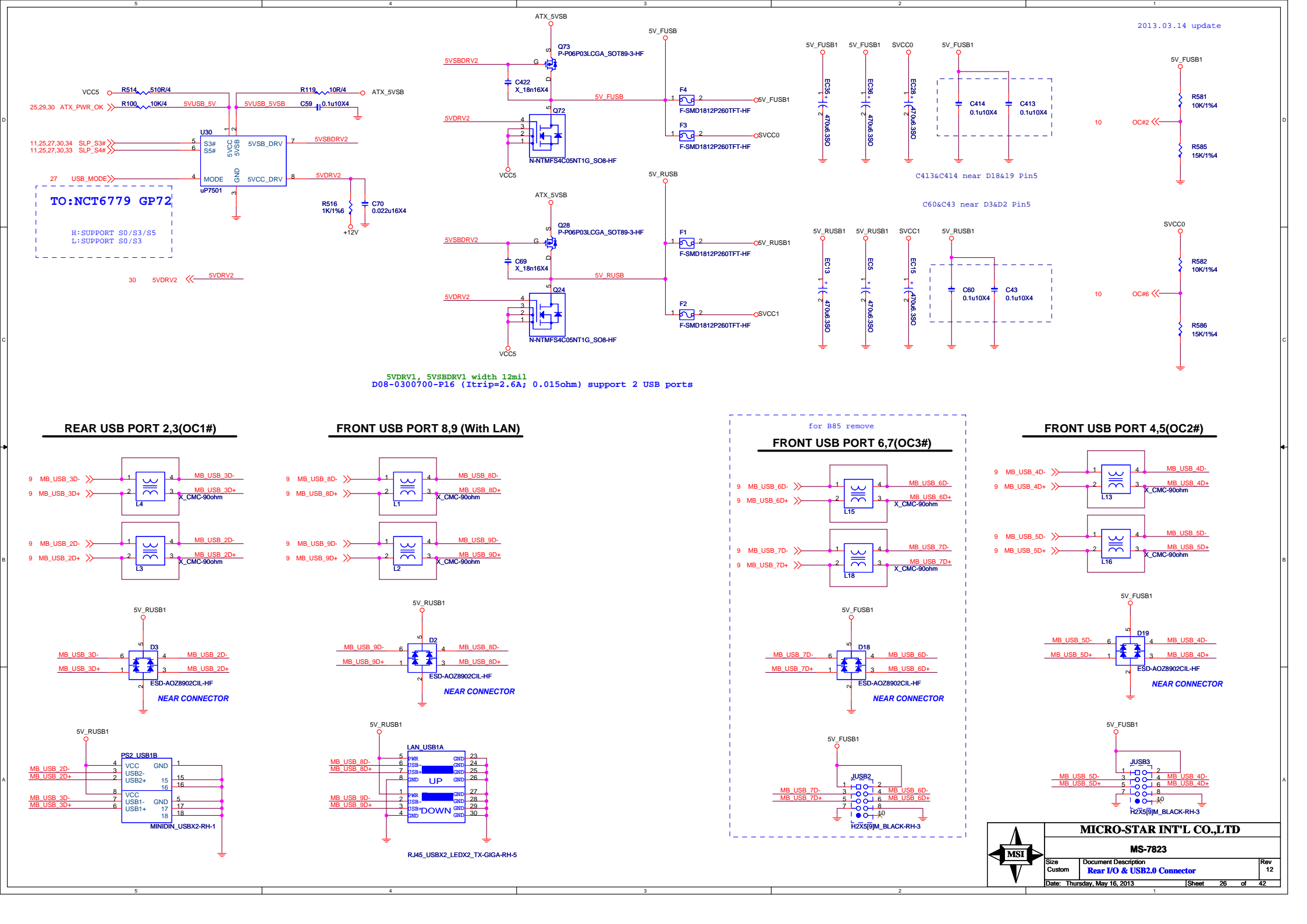
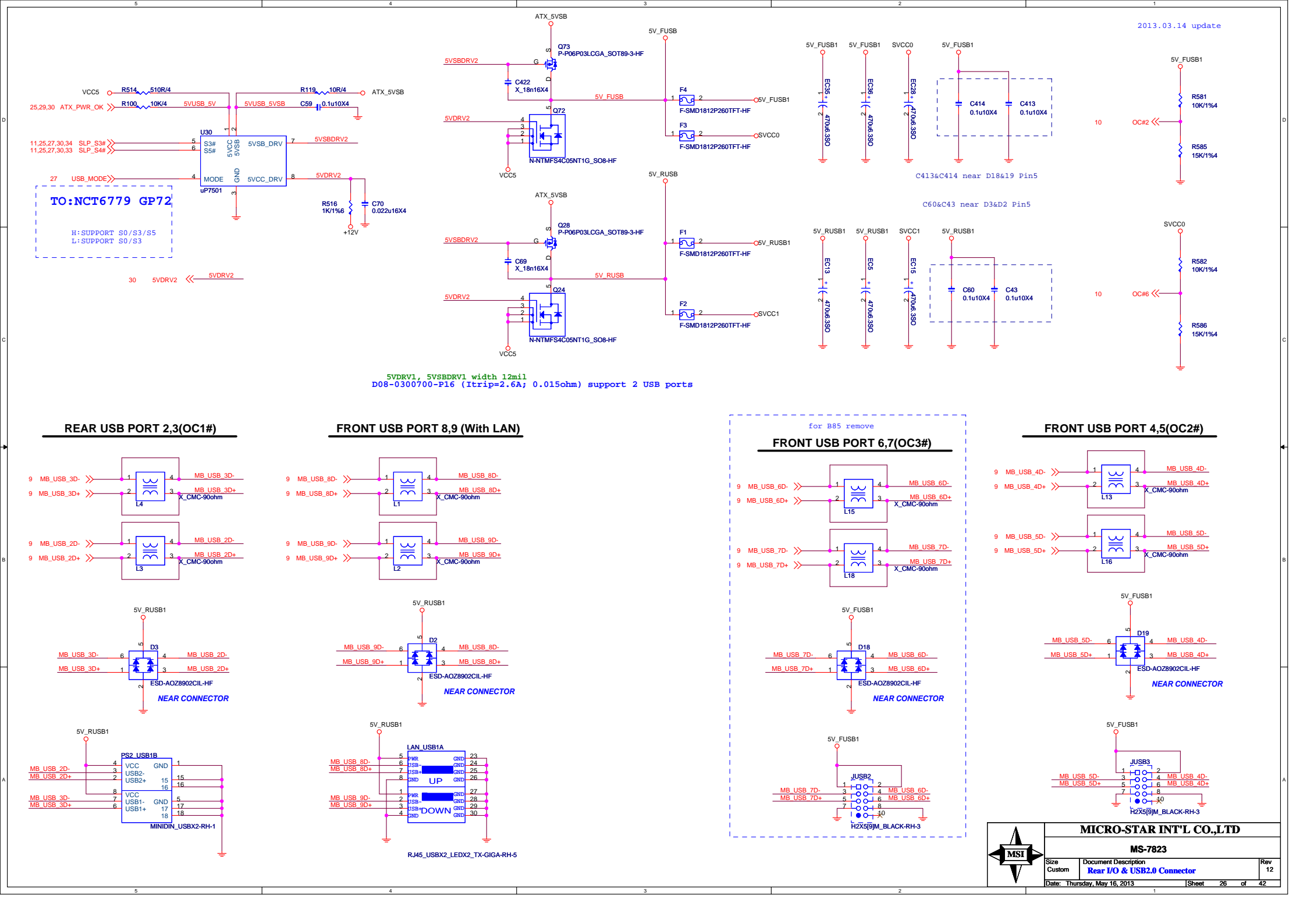
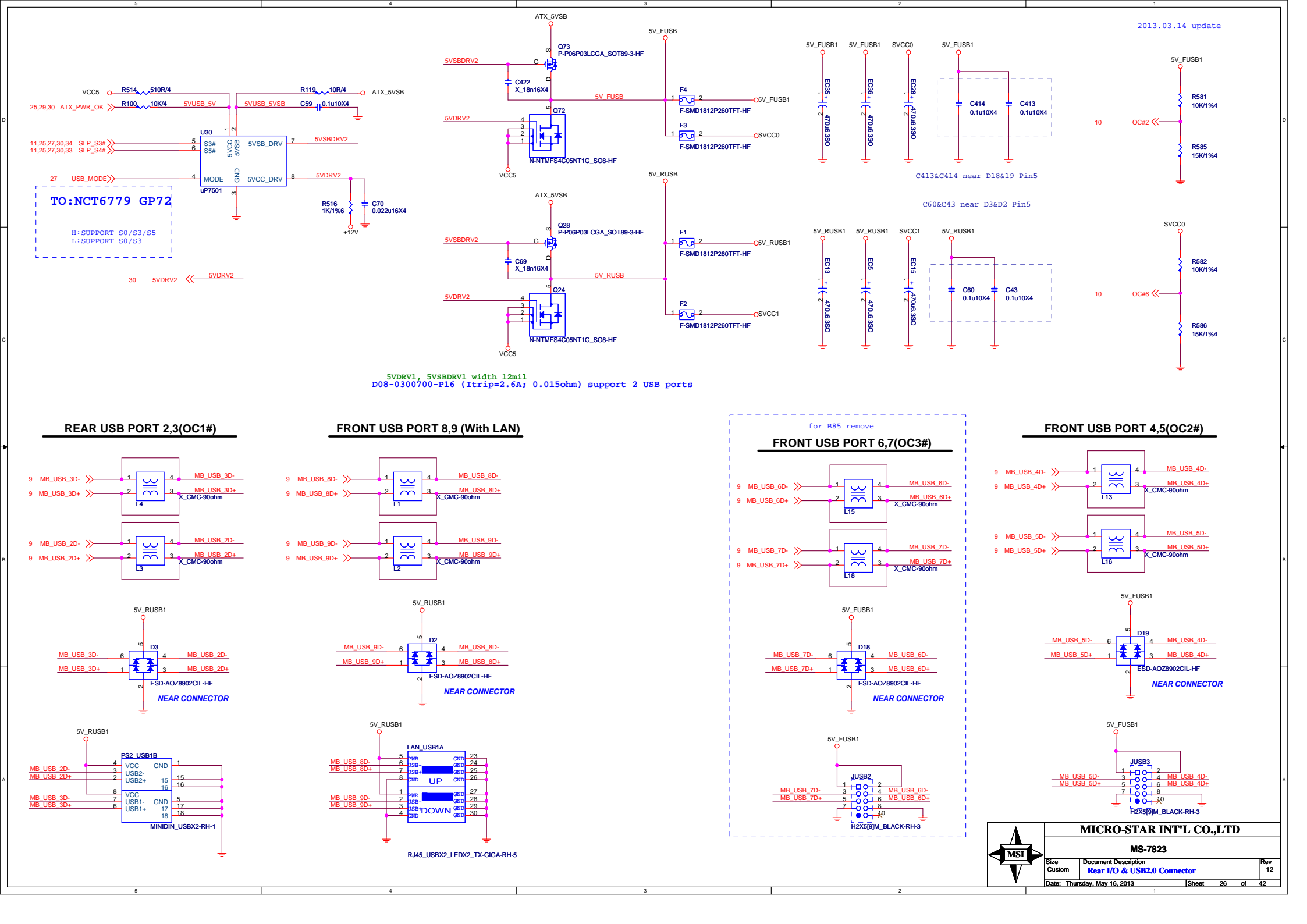
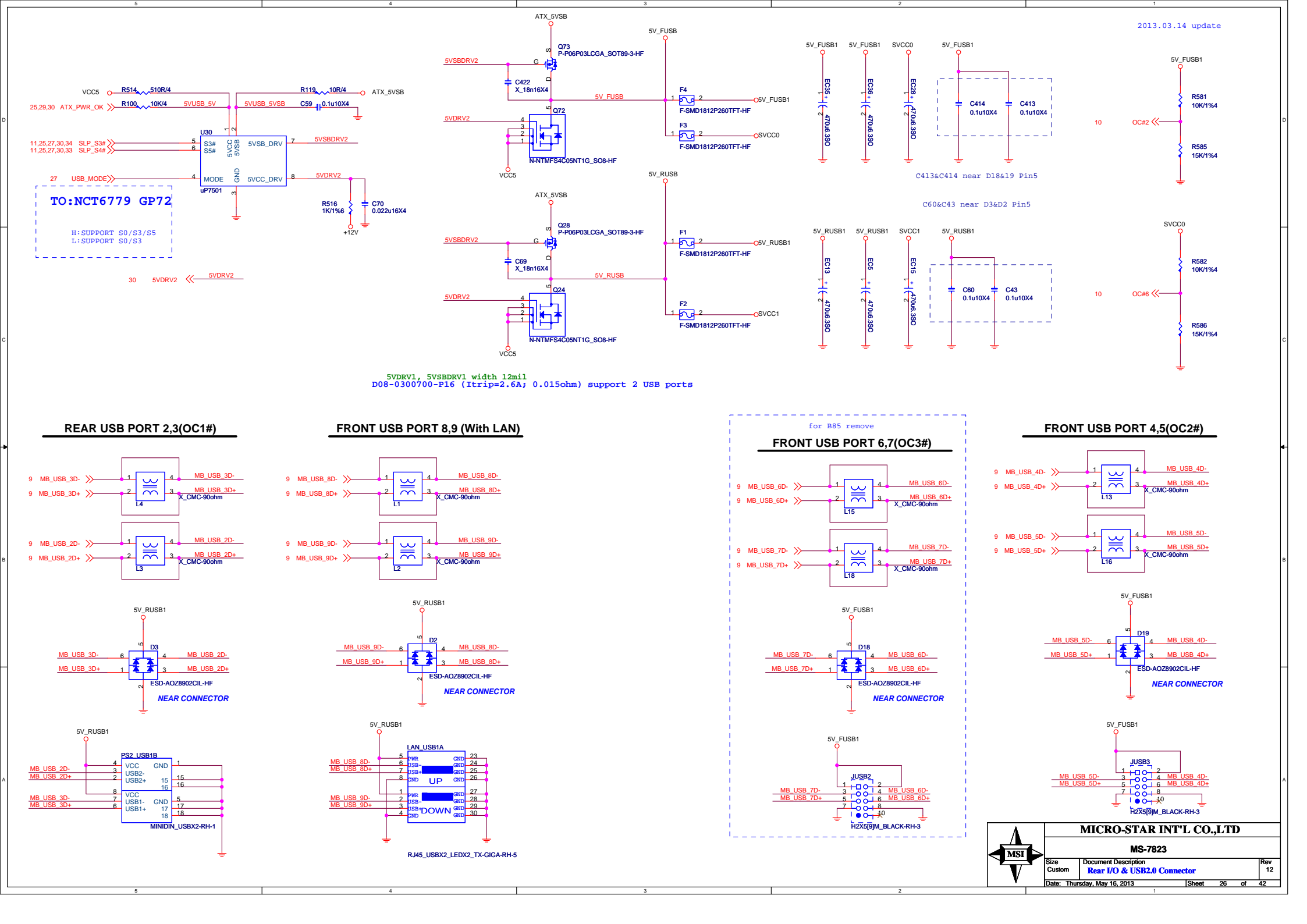
**MS-7823**

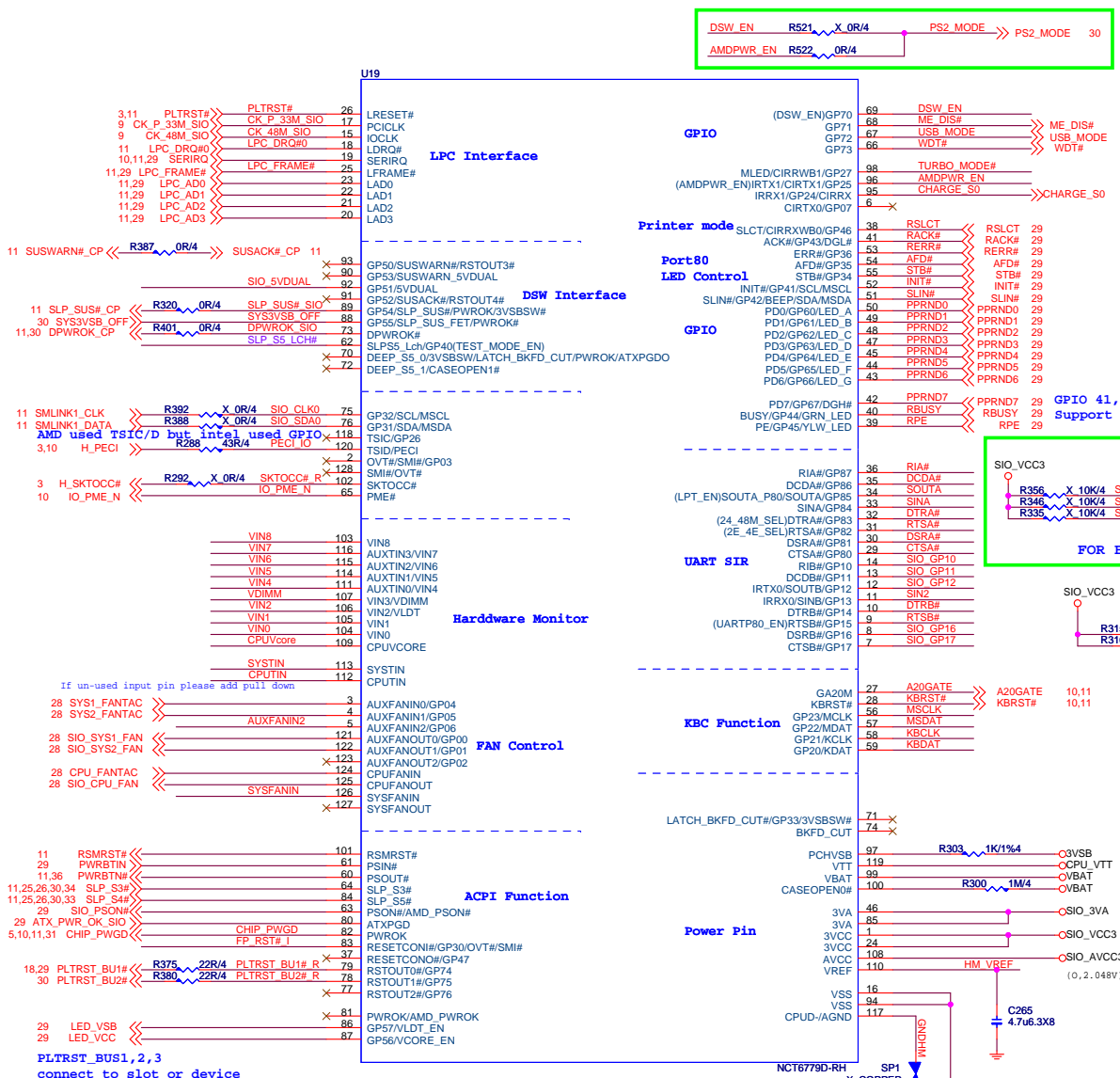
Size Custom Document Description Date: Thursday, May 16, 2013 Sheet 26 of 42

Rev 12

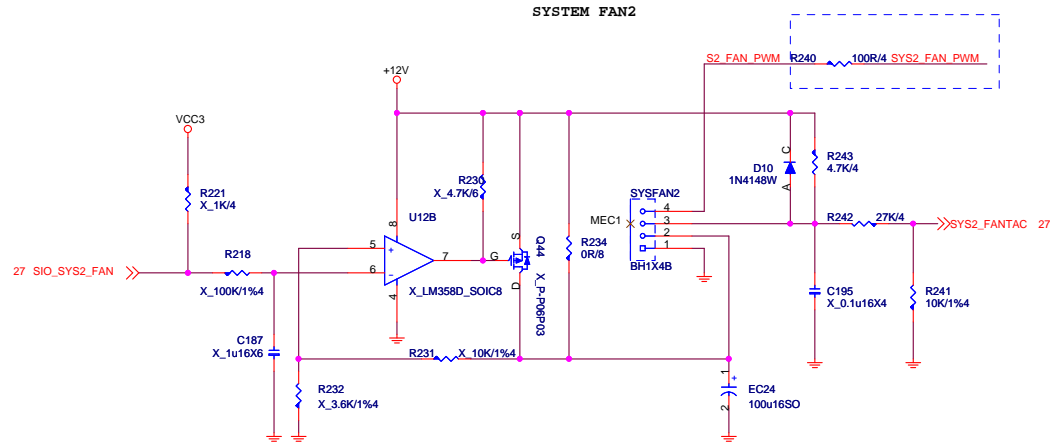
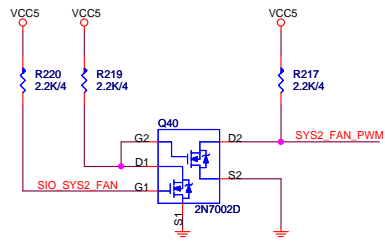
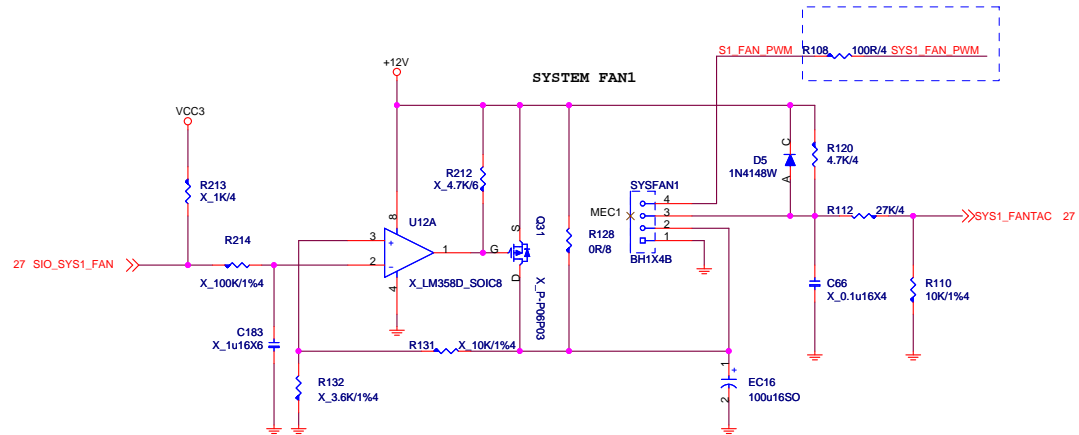
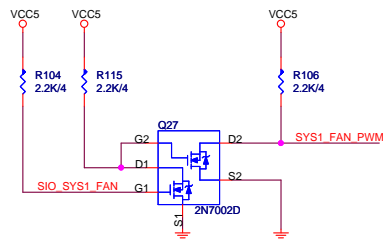
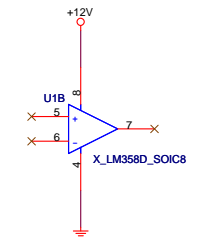
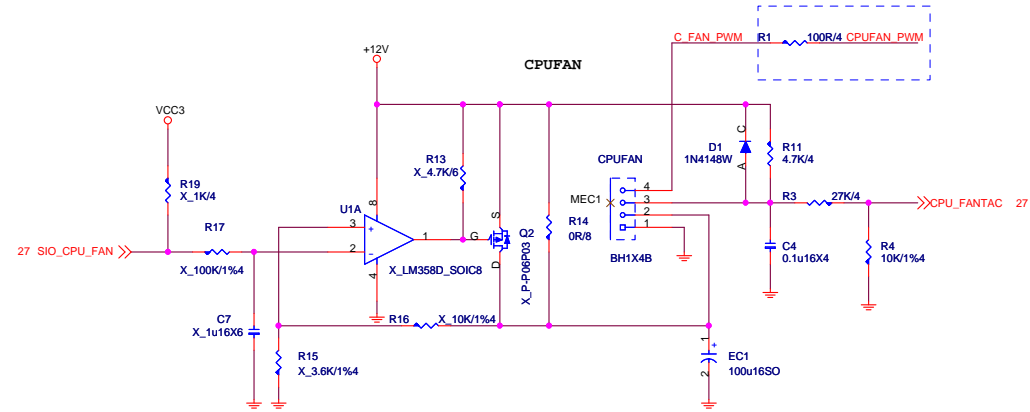
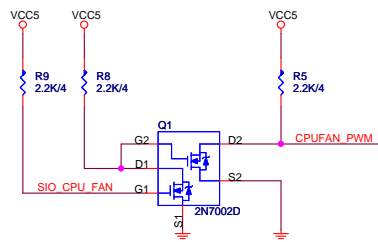
Micro-Star Intl Co., Ltd

Rear I/O & USB2.0 Connector





# FAN-COUNTROL CIRCUIT







**5V DIMM FOR DDR**

VCC5  $\text{R35 } 510\text{R}/4$   $\text{R41 } 10\text{K}/4$  5V DIMM 5V 5V DIMM 5VSB C31  $0.1\mu\text{10X4}$  ATX\_5VSB

25,26,29 ATX\_PWR\_OK 11,25,26,27,34 SLP\_S3# 11,25,26,27,33 SLP\_S4#

U5 S3# S5# 5V5B 5V5B 5V5B DRV 5V5BDRV1 7 5V5BDRV1 C33  $18\text{n16X4}$  Q4 P-P06P03LPGA\_SOT89-3-HF

MODE uP7501 GND 5V5B\_DRV 8 5V5BDRV1 R42  $1\text{K}/1\%6$  C37  $0.022\mu\text{16X4}$  VCC5 Q3 N-NTMFS4C08NT1G\_S08-HF

7501 Mode  
H:Support S0/S3/S5  
L:Support S0/S3

35 5V5BDRV1  $\leftarrow$  5V5BDRV1 C27  $0.1\mu\text{10X4}$

[illegible][illegible]

**3.389V**

ATX\_5VSB

C356  
1u6.3X4

R457  
47K/4

U23  
UP0111AMA5

VIN

VOUT

EN

GND

FB

X\_0.1u10X4

3VA FB

R422  
10K/1%4

C353  
4.7u6.3X8

3VA

C341

3.389V

R418  
3.09K1%4

把3VA調高到3.389V

for NCT6779 Ver.C not stuff

3VA

R442  
X\_10K/4

C346  
X\_10u6.3X6

ATX\_5VSB

R492  
X\_10K/4

3VA

R486  
499/1%4

DPWROK\_CP

DPWROK\_CP 11,27

Q67  
X\_2N3904

R487  
10K/4

C383  
X\_1u6.3X4

Q62

B

C

X\_2N3904

R454  
X\_4.12K/1%4

C361  
X\_4.7u6.3X8

3.389V分壓=0.7V  
2.55V分壓=0.528V

FOR DPWROK跟3VA的POWER DOWN的時序 (S5-->G3)

把PCH DPWRROK\_CP的PUULL HIGH移到這裡

DPWROK需要加一顆pull down 10k電阻，可解工廠端BAT 電流過大問題

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.

ATX\_5VSB

R54 47K/4

C39 1u6.3X6

G2

D1

D2 5VDRV1\_5V

S2

G1

Q16 2N7002D

S1

R55 47K/4

C40 1u6.3X6

GPIO13 from PCH

TO ALL PCIE SLOT RESET#

11 PCH\_GPIO13 >>> PCH\_GPIO13

27 PLTRST\_BU2# >>> PLTRST\_BU2#

U20

X\_NC7SZ08M5X\_SOT23-5

PE\_S\_RESET\_N 15,16

R364 0R/4

PCIE\_SLOT\_RESET\_N

from SIO RESET BUS2

MICRO STAR INT'L CO. LTD.

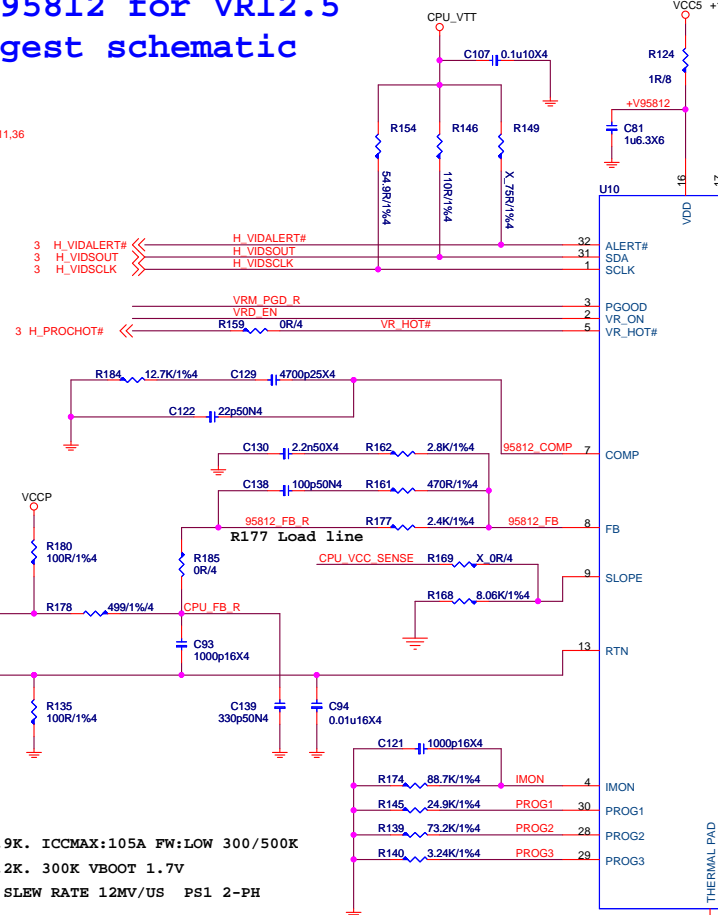
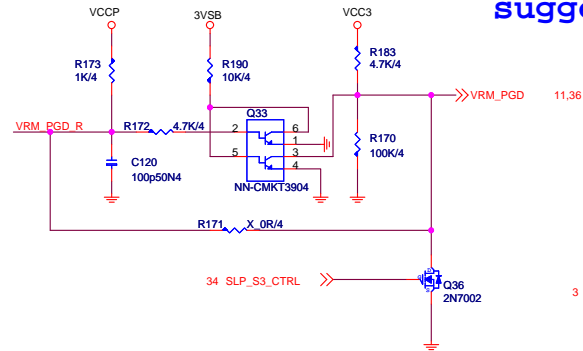


MS-7823

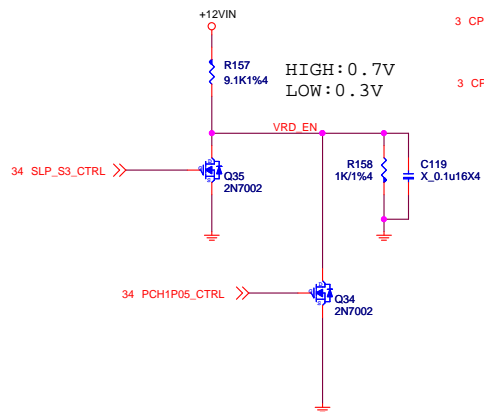
Size Custom	Document Description <b>ACPI controller UPI</b>	Rev 12
Date: Thursday, May 16, 2013		Sheet 30 of 42

# ISL95812 for VR12.5 suggest schematic

VCCP: 95W  
IccMAX: 95A  
TDC: 55A  
VID1: 1.8V



VCORE power on by s3 and 12v



R145 TO 24.9K. ICCMAX:105A FW:LOW 300/500K  
R139 TO 73.2K. 300K VBOOT 1.7V  
R140 3.24K SLEW RATE 12MV/US PS1 2-PH

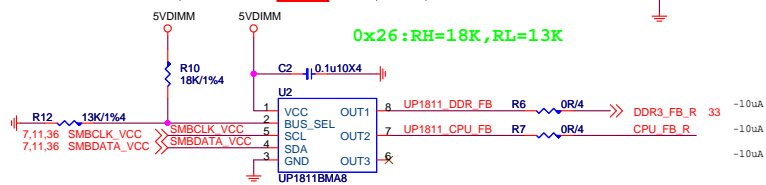
IC thermal pad 8 VIA  
connect GND lay

Since Idroop also sets the overcurrent protection level, it is recommended to first scale Idroop based on OCP requirement, then select an appropriate Idroop value to obtain the desired load line slope.

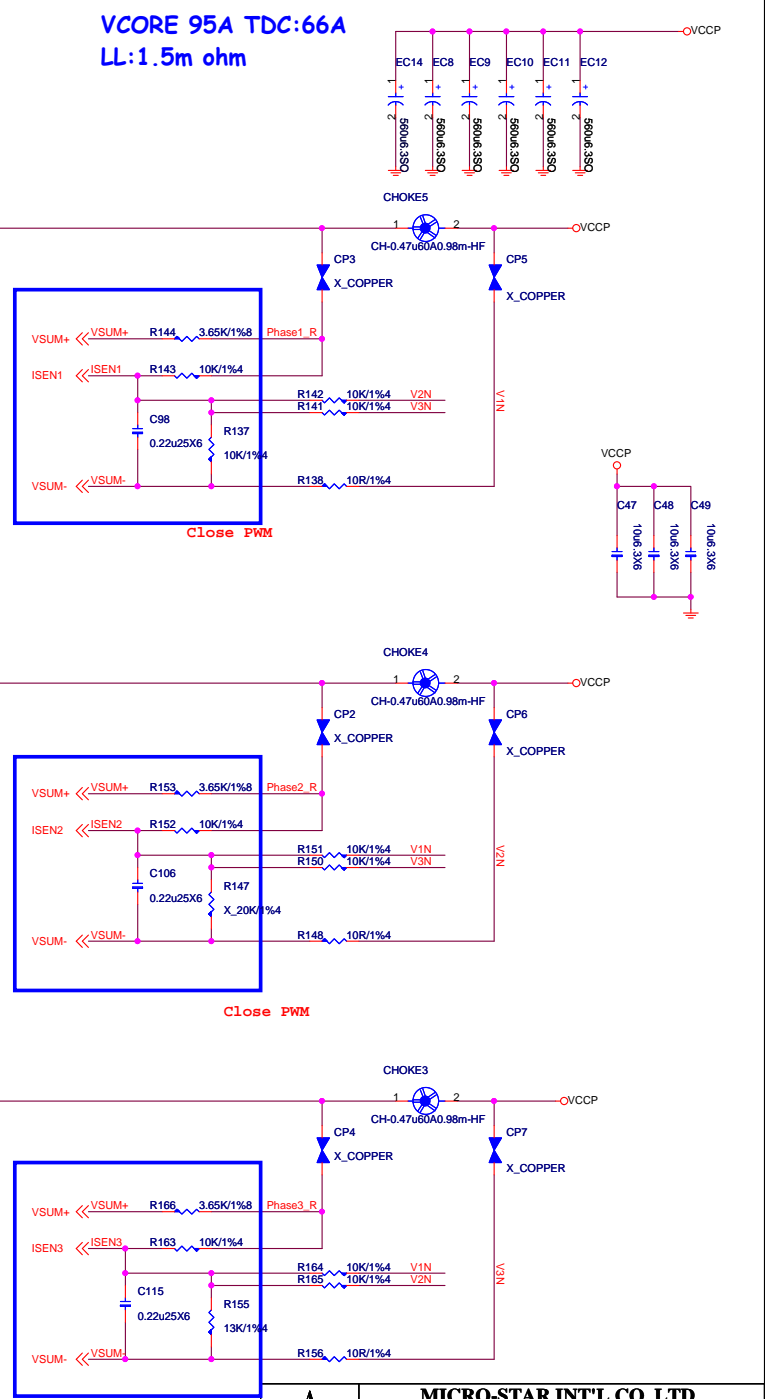
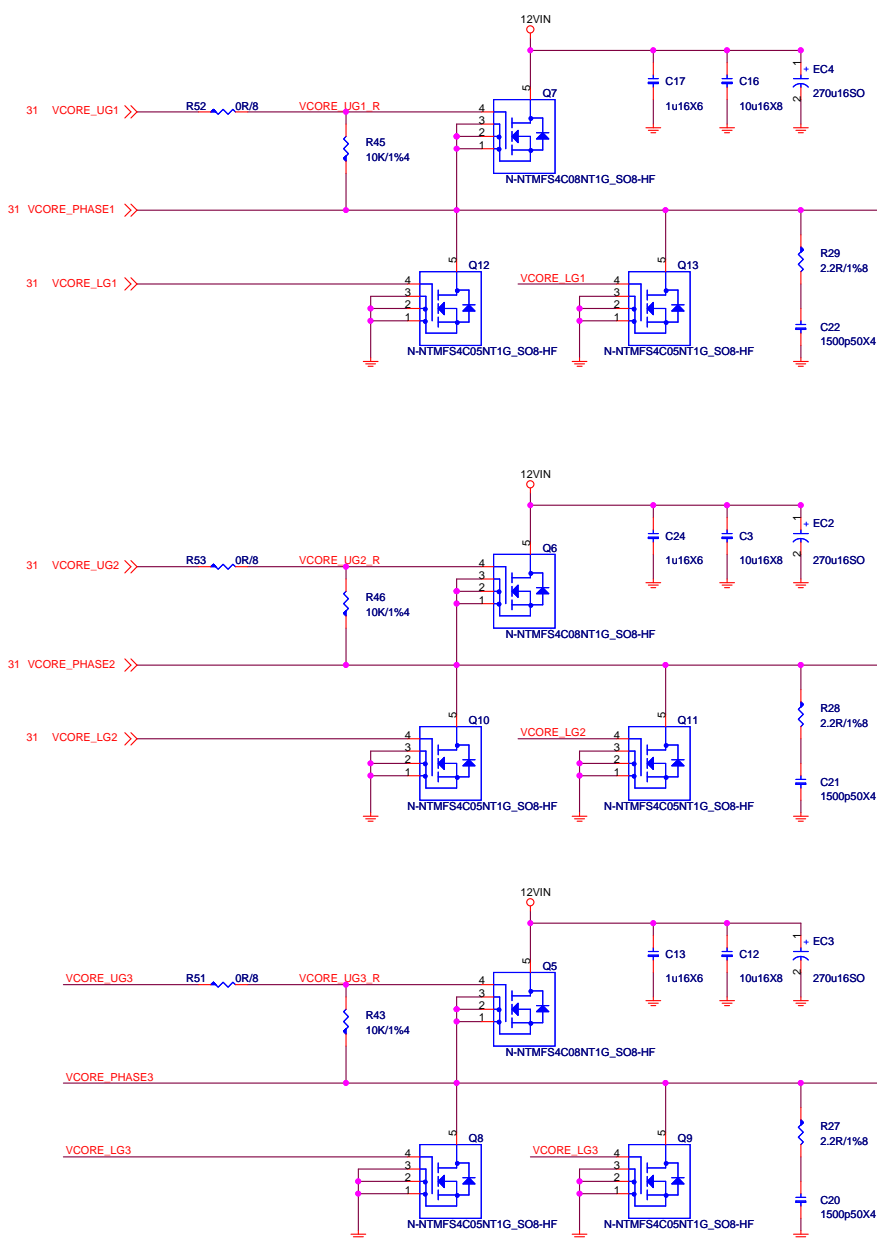
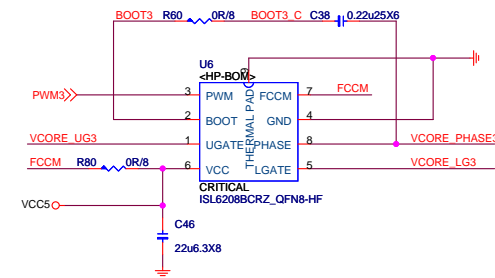
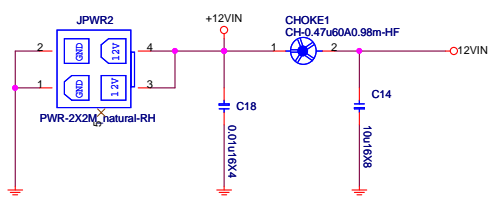
## UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%


0x26: RH=18K, RL=13K



OUTPUT CURRENT: ICCMAX 95A  
I<sub>rms</sub> = 15.76A  
Input Cap 5.08A\*3= 15.24A



VCORE 95A TDC:66A  
LL:1.5m ohm



**MICRO-STAR INT'L CO.,LTD**

**MS-7823**

Size	Document Description	Rev
Custom	30 ISL6208B 3-Phase+MOS CPU	12
Date:	Thursday, May 16, 2013	Sheet 32 of 42

# DDR Power:1.5V

DDR3\_1.5V 4.2A+12A+1.115A+5.921A=23.236A

4.2A FOR CPU

12A FOR 4DIMM

1.115A FOR VTT\_DDR

5.921A FOR PCH

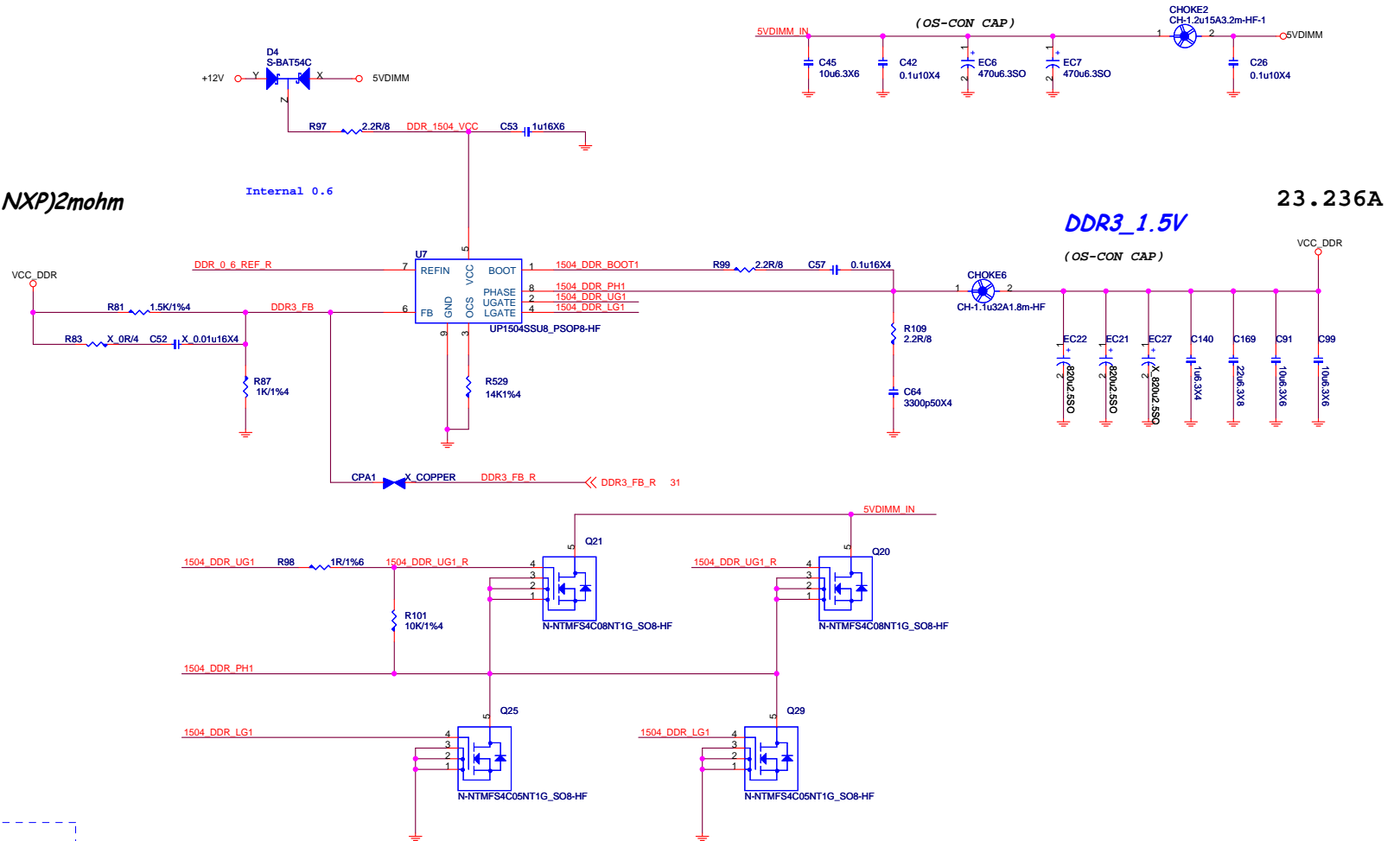
OCP 23.236A\*1.5=34.845A

OCP=[20uA\*Rocs(R320)]/4\*Rdson(Low side NXP)2mohm

R529=14K ohm

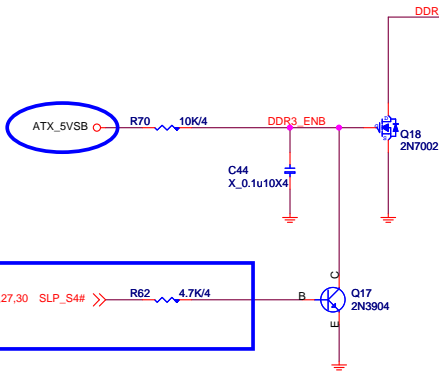
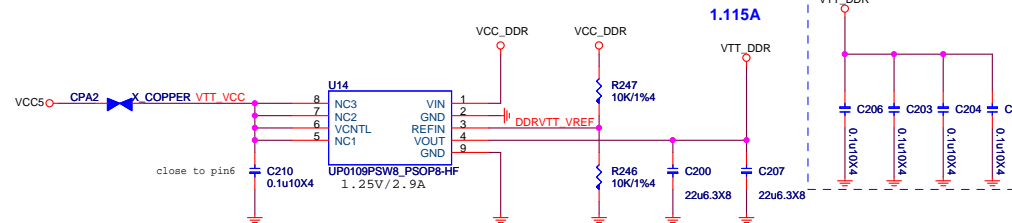
Iripple=10.64807288A

4.7\*2\*1=9.4A



## DDR VTT Power

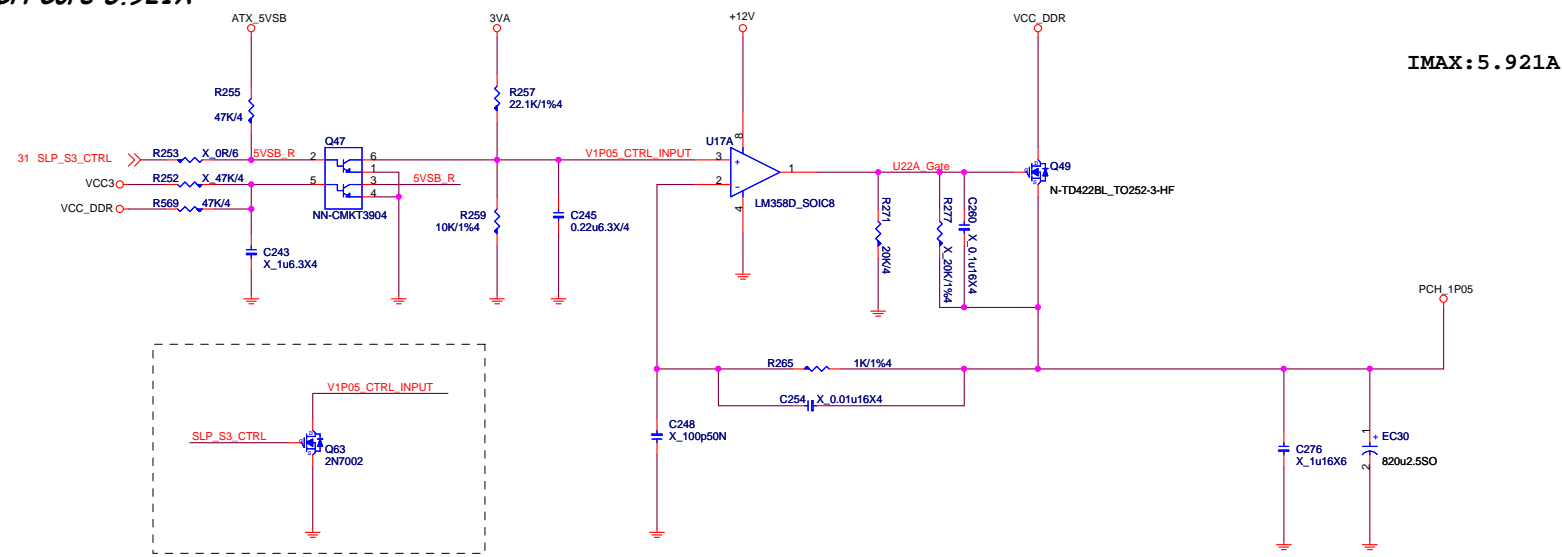
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



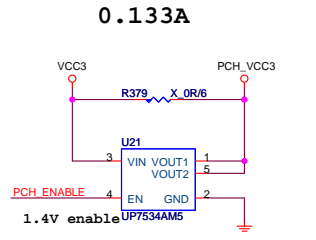
P.S. Only for meet Intel power down sequence.

MSI		
MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size	Document Description	Rev
Custom	DDR Power - UPI504S 2-Phase MOS	12
Date:	Thursday, May 16, 2013	Sheet 33 of 42

PCH Power:1.05V  
PCH Core 5.921A

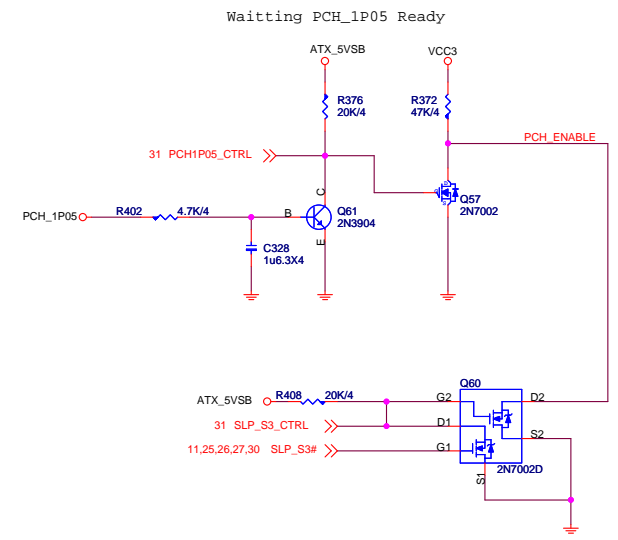


PCH Power:3.3V

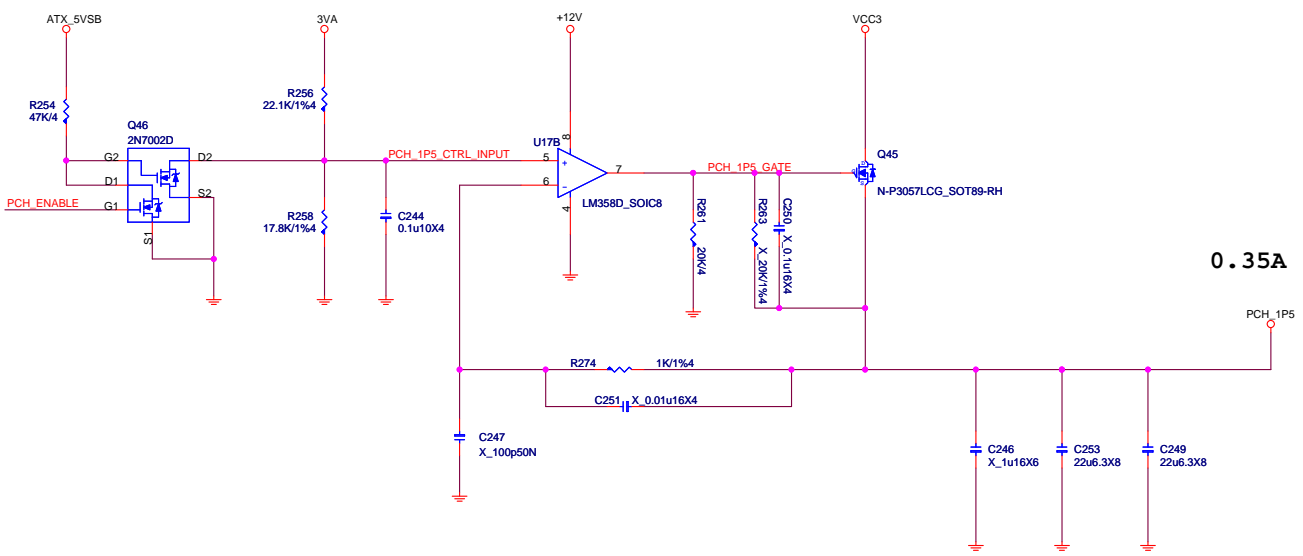


VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH

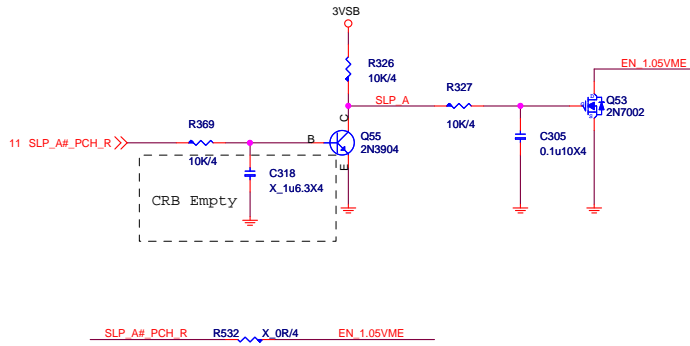
PCH Power:1.5V



VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH

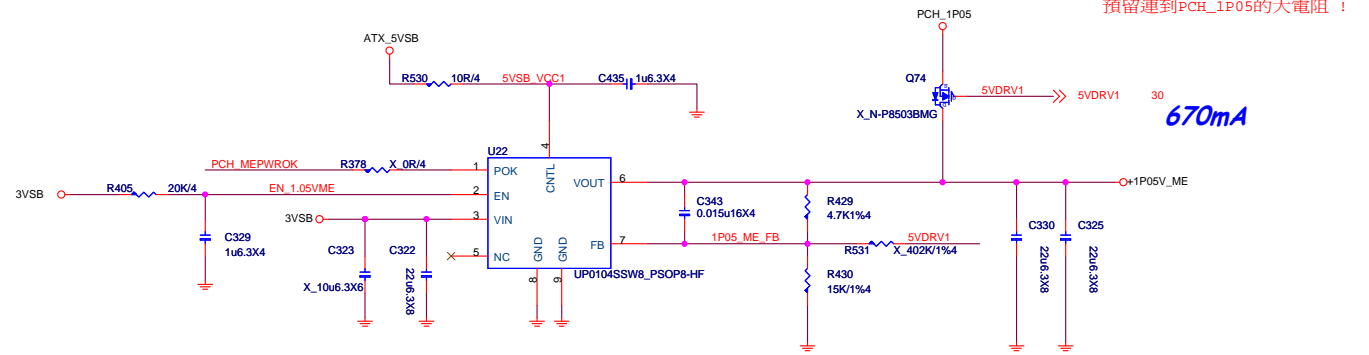


## SLP\_A

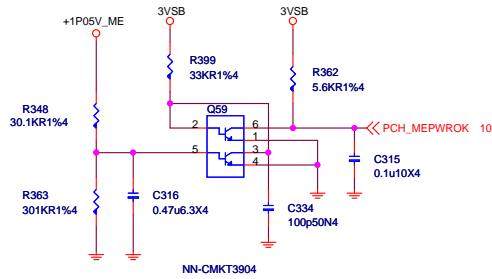


## ME Power Control

## +1.05V\_ME(VCCIO\_ME)

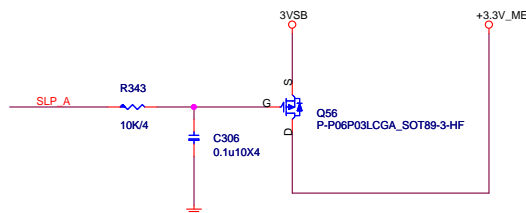


## PCH\_MEPWROK

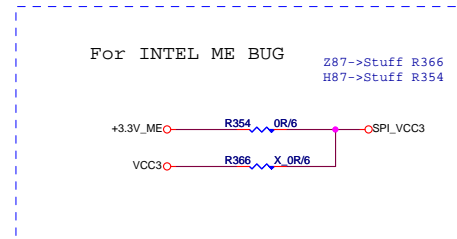


VccASW active to APWROK high 1ms

## +3.3V\_ME



APWROK falling to VccASW falling 40ns



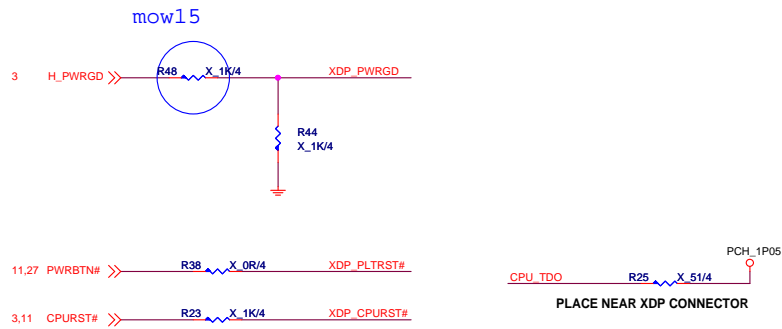
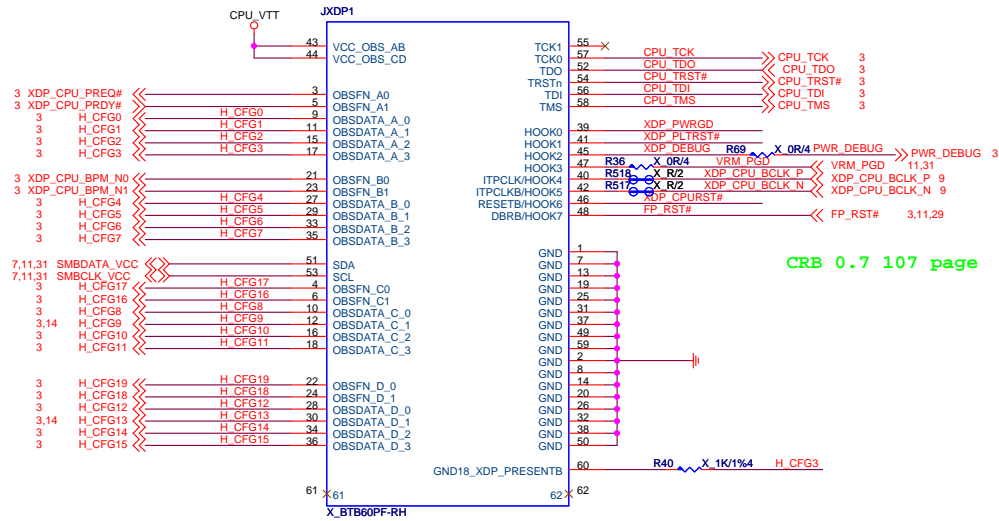
MICRO-STAR INT'L CO.,LTD

MS-7823

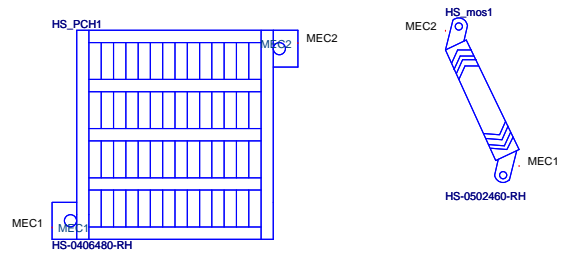
Size Custom	Document Description <b>ME POWER</b>	Rev 12
Date: Thursday, May 16, 2013	Sheet 35 of 42	



# **Reserve debug port 5020**

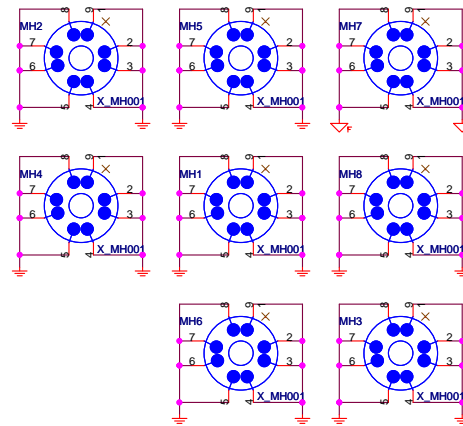


## HEATSINK



PK0-0782312-G37, 精成, 23, 寶安恩思邁廠 (MSIS)  
PK0-0782312-E48, 競華, 23, 寶安恩思邁廠 (MSIS)

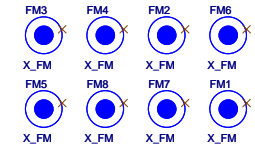
## Mounting Holes



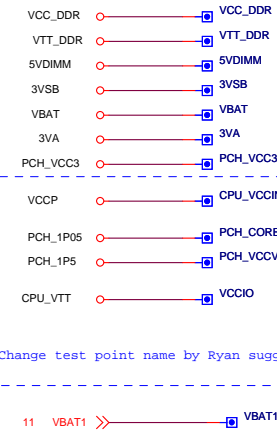
## Simulation



## Optical Fiducial Marks-120



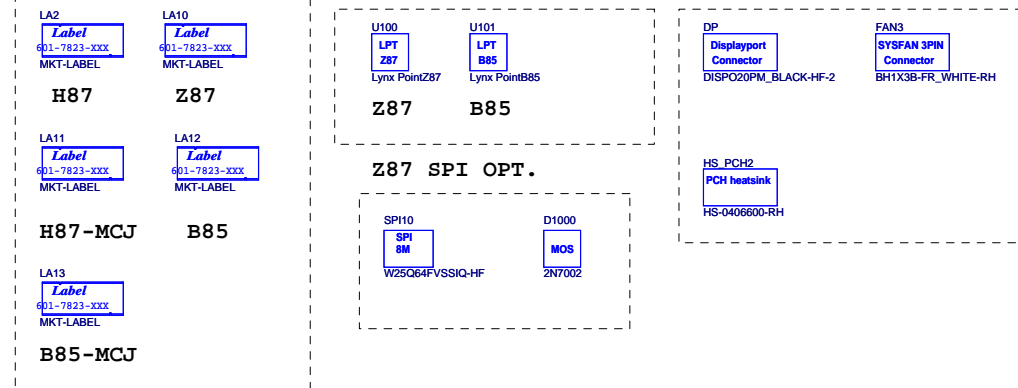
## Test point



## Label OPT.

## Chip OPT.

## MCJ OPT.



## MS-7823-1.2 主BOM為H87

OPT	Configure	BOM	Function	GPIO Setting(GP10/GP11/GP12)
	H87M-G43		MS-7823 11 H87 H87M-G43, H87, LGA1150, 4DDR3, 2PCI-Ex16, 2PCI-Ex1 6SATA3, 4USB3, HD Audio, Gb LAN, HDMI, DP, DVI, D-Sub	0, 0, 0
	Z87M-G43		MS-7823 11 OPT:E Z87 Z87M-G43, Z87, LGA1150, 4DDR3, 2PCI-Ex16, 2PCI-Ex1 6SATA3, 4USB3, HD Audio, Gb LAN, HDMI, DP, DVI, D-Sub	0, 0, 0
	H87M-S01 (MCJ)		MS-7823 12 H87 H87M-S01, H87, LGA1150, 4DDR3, 2PCI-Ex16, 2PCI-Ex1 6SATA3, 4USB3, HD Audio, Gb LAN, DP, DVI, D-Sub	1, 0, 0
	B85M-G43		MS-7823 11 OPT:G B85 B85M-G43, B85, LGA1150, 4DDR3, 2PCI-Ex16, 2PCI-Ex1 4SATA3, 4USB3, HD Audio, Gb LAN, HDMI, DP, DVI, D-Sub	0, 0, 0
	B85M-S01 (MCJ)		MS-7823 11 OPT:H B85 B85M-S01, B85, LGA1150, 4DDR3, 2PCI-Ex16, 2PCI-Ex1 4SATA3, 4USB3, HD Audio, Gb LAN, DP, DVI, D-Sub	1, 0, 0

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1



MICRO-STAR INT'L CO.,LTD		
MS-7823		
Size Custom	Document Description EMI CAP	Rev 12
Date: Thursday, May 16, 2013		Sheet 38 of 42